NOVOSENSE
纳芯微电子

NSI8200

High Reliability Bidirectional I²C Isolators

Datasheet (EN) 1.1

Product Overview

The NSI8200 devices are high reliability bidirectional isolators that are compatible with I²C interface. The NSI8200 devices are safety certified by UL1577 support several withstand isolation voltages (3.75kV$_{RMS}$, 5kV$_{RMS}$, 8kV$_{RMS}$), while providing high electromagnetic immunity and low emissions at low power consumption. The I²C clock frequency of the NSI8200 is up to 2MHz, and the common-mode transient immunity (CMTI) is up to 150kV/μs. Wide supply voltage of the NSI8200 device support to connect with most digital interface directly, easy to do the level shift. High system level EMC performance enhance reliability and stability of use.

Key Features

- Up to 5000V$_{RMS}$ Insulation voltage
- I²C Clock rate: up to 2MHz
- Power supply voltage: 2.5V to 5.5V
- High CMTI: 150kV/μs
- Chip level ESD: HBM: ±6kV
- High system level EMC performance:
  - Enhanced system level ESD, EFT, Surge immunity
- Low power consumption: 3.35mA/ch (2 MHz)
- Operation temperature: -40℃~125℃
- RoHS-compliant packages:
  - SOP8
  - SOW16
  - SOWW8

Safety Regulatory Approvals

- UL recognition:
  - SOP8: 3750V$_{RMS}$ for 1 minute per UL1577
  - SOW16: 5000V$_{RMS}$ for 1 minute per UL1577
  - SOWW8: 8000V$_{RMS}$ for 1 minute per UL1577
- CQC certification per GB4943.1-2011
- CSA Component Acceptance Notice 5A
- DIN VDE V 0884-11:2017-01

Applications

- Power over ethernet
- Isolated I²C, SMBus, or PMBus interface
- I²C level shifting
- Battery Management

Device Information

Part Number	*Package*	*Body Size (NOM)*
NSI8200-DSPR	SOP8	4.90mm × 3.90mm
NSI8200-DSWR	SOW16	10.30mm × 7.50mm
NSI8200-DSWWAR	SOWW8	6.25mm × 13.60mm

Functional Block Diagrams

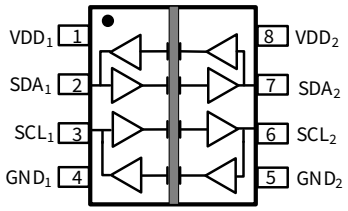

Figure 1. NSI8200-DSPR & NSI8200-DSWWAR Block Diagram

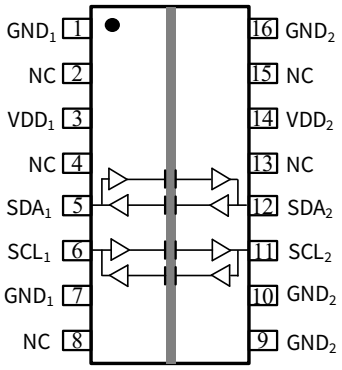

Figure 2. NSI8200-DSWR Block Diagram

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1. Pin Configuration and Functions

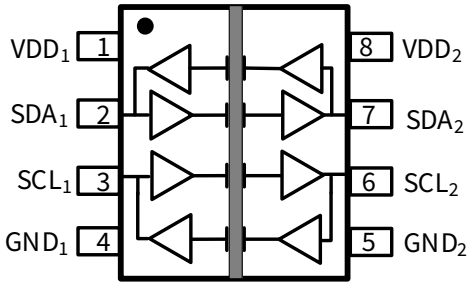


Figure 1. 1 NSI8200-DSPR & NSI8200-DSWWAR Package

Table 1. 1 NSI8200-DSPR & NSI8200-DSWWAR Pin Configuration and Description

NSI8200-DSPR & NSI8200-DSWWAR PIN NO.	*SYMBOL*	*DESCRIPTION*
1	VDD_1	Power Supply for Isolator Side 1
2	SDA_1	Serial data input /output, Side 1
3	SCL_1	Serial clock input /output, Side 1
4	GND_1	Ground 1, the ground reference for Isolator Side 1
5	GND_2	Ground 2, the ground reference for Isolator Side 2
6	SCL_2	Serial clock input /output, Side 2
7	SDA_2	Serial data input /output, Side 2
8	VDD_2	Power Supply for Isolator Side 2

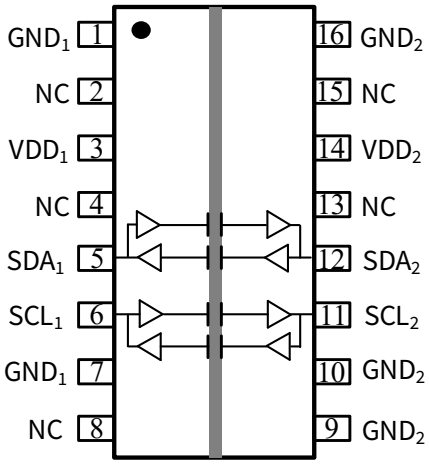


Figure 1. 2 NSI8200-DSWR Package

Table 1. 2 NSI8200-DSWR Pin Configuration and Description

NSI8200-DSWR PIN NO.	*SYMBOL*	*DESCRIPTION*
1	GND_1	Ground 1, the ground reference for Isolator Side 1
2,4,8,13,15	NC	No Connection
3	VDD_1	Power Supply for Isolator Side 1
5	SDA_1	Serial data input /output, Side 1
6	SCL_1	Serial clock input /output, Side 1
7	GND_1	Ground 1, the ground reference for Isolator Side 1
9	GND_2	Ground 2, the ground reference for Isolator Side 2
10	GND_2	Ground 2, the ground reference for Isolator Side 2
11	SCL_2	Serial clock input /output, Side 2
12	SDA_2	Serial data input /output, Side 2
14	VDD_2	Power Supply for Isolator Side 2
16	GND_2	Ground 2, the ground reference for Isolator Side 2

2. Absolute Maximum Ratings

PARAMETER	SYMBOL	MIN	MAX	UNIT
Power Supply Voltage	VDD_1, VDD_2	-0.5	6.5	V
Maximum Input Voltage	SCL_x, SDA_x	-0.4	VDD+0.4[1]	V
Maximum Input Pulse Voltage	SCL_x, SDA_x	-0.8	VDD+0.8[2]	V
Output current	I_O	-15	15	mA
Ambient Temperature	T_A	-40	125	℃
Junction Temperature	T_J	-40	150	℃
Storage Temperature	T_{stg}	-65	150	℃

1. The maximum voltage must not exceed 6.5V.
2. Pulse width should be less than 100ns, and the duty cycle should be less than 10%.

3. ESD Ratings

	Ratings	Value	Unit
Electrostatic discharge	Human body model (HBM), per AEC-Q100-002-RevD ● All pins	±6	kV
	Charged device model (CDM), per AEC-Q100-011-RevB ● All pins	±2	kV

4. Recommended Operating Conditions

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Power Supply Voltage	VDD_1, VDD_2	2.5		5.5	V
Operating Temperature	T_A	-40		125	℃
Side1 High Level Input Voltage	V_{IH1}	0.5		0.63	V
Side1 Low Level Input Voltage	V_{IL1}	0.44		0.56	V
Side2 High Level Input Voltage	V_{IH2}	0.7*VDD_2			V
Side2 Low Level Input Voltage	V_{IL2}			0.3*VDD_2	V
Data Rate	DR			2	MHz

5. Thermal Characteristics

PARAMETER	Symbol	SOW16	SOP8	SOWW8	UNIT
Junction-to-Air Thermal Resistance	$R_{\theta JA}$	86.5	137.7	78.9	℃/W
Junction-to-case (top) thermal resistance	$R_{\theta JC(top)}$	49.6	54.9	41.6	℃/W
Junction-to-board thermal resistance	$R_{\theta JB}$	49.7	71.7	43.6	℃/W

6. Specifications

6.1. Electrical Characteristics

(VDD_1=2.5V~5.5V, VDD_2=2.5V~5.5V, T_A =-40℃ to 125℃. Unless otherwise noted, Typical values are at VDD_1= VDD_2= 3.3V, T_A= 25℃)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT	COMMENT
Power on Reset	VDD_{POR}		2.2		V	POR threshold as during power-up
	VDD_{HYS}		0.1		V	POR threshold Hysteresis
Start Up Time after POR	t_{START}		40		μs	
Common Mode Transient Immunity	CMTI	±100	±150		kV/μs	See Figure 6.9
Input leakage current	I_{LI}	-15		15	μA	V_{SDA1}= V_{SCL1}=VDD_1, V_{SDA2}= V_{SCL2}=VDD_2
Side 1 Logic Level						
Input Threshold	V_{ILT1}	440		560	mV	Input Threshold at falling edge
	V_{IHT1}	500		630	mV	Input Threshold at rising edge
	V_{IT_HYS1}		50	130	mV	Input Threshold Hysteresis
Low Level Output Voltage	V_{OL1}	650		800	mV	$R_{PULL\ UP}$=1kΩ
Low-level output voltage to high-level input voltage threshold difference	ΔV_{OIT1}	70	150		mV	
Side 2 Logic Level						
High Level Input Voltage	V_{IH2}	0.7* VDD_2			V	
Low Level Input Voltage	V_{IL2}			0.3* VDD_2	V	
Low Level Output Voltage	V_{OL2}			500	mV	I_{OL} ≤ 30mA

(VDD_1=5V± 10%, VDD_2=5V± 10%, T_A =-40℃ to 125℃. Unless otherwise noted, Typical values are at VDD_1= VDD_2= 5V, T_A = 25℃)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT	COMMENT
Supply current	I_{DD1}(Q0)		5.40	6.6	mA	All Input 0V
	I_{DD2}(Q0)		4.32	5.2	mA	
	I_{DD1}(Q1)		2.94	3.8	mA	All Input at supply
	I_{DD2}(Q1)		1.89	2.7	mA	
	I_{DD1}(2M)		3.21	4.6	mA	All Input with 2MHz, C_{L1}= C_{L2}=10pF
	I_{DD2}(2M)		2.37	4.1	mA	
Data Rate	DR			2	MHz	
Propagation Delay	t_{PLH12}		39	59	ns	See Figure 6.7, R_1=1.5kΩ, R_2=150Ω, C_{L1}= C_{L2}=10pF
	t_{PHL12}		38	57	ns	See Figure 6.7, R_1=1.5kΩ, R_2=150Ω, C_{L1}= C_{L2}=10pF
	t_{PLH21}		70.5	106	ns	See Figure 6.7, R_1=1.5kΩ, R_2=150Ω, C_{L1}= C_{L2}=10pF
	t_{PHL21}		36	54	ns	See Figure 6.7, R_1=1.5kΩ, R_2=150Ω, C_{L1}= C_{L2}=10pF
Pulse Width Distortion	PWD_{12}		1	53	ns	$\lvert t_{PHL12} - t_{PLH12} \rvert$
	PWD_{21}		35	53	ns	$\lvert t_{PHL21} - t_{PLH21} \rvert$
Falling Time	t_{f1}		5.9	10	ns	R_1=1.5kΩ, R_2=150Ω, C_{L1}=40pF, C_{L2}=400pF, 0.7*VDD_1 to 0.3*VDD_1
			11.5	19		R_1=1.5kΩ, R_2=150Ω, C_{L1}=40pF, C_{L2}=400pF, 0.9*VDD_1 to 900mV
	t_{f2}		7.4	12	ns	R_1=1.5kΩ, R_2=150Ω, C_{L1}=40pF, C_{L2}=400pF, 0.7*VDD_2 to 0.3*VDD_2
			16.8	26		R_1=1.5kΩ, R_2=150Ω, C_{L1}=40pF, C_{L2}=400pF, 0.9*VDD_1 to 400mV

(VDD_1=3.3V± 10%, VDD_2=3.3V± 10%, T_A=-40℃ to 125℃. Unless otherwise noted, Typical values are at VDD_1= VDD_2= 3.3V, T_A = 25℃)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT	COMMENT
Supply current	I_{DD1}(Q0)		5.4	6.5	mA	All Input 0V
	I_{DD2}(Q0)		4.2	5.1	mA	
	I_{DD1}(Q1)		2.8	3.7	mA	All Input at supply
	I_{DD2}(Q1)		1.8	2.6	mA	
	I_{DD1}(2M)		3.6	4.7	mA	All Input with 2MHz, C_{L1}= C_{L2}=10pF

	I_{DD2}(2M)		3.1	4	mA	
Data Rate	DR			2	MHz	
Propagation Delay	t_{PLH12}		38.9	59	ns	See Figure 6.7, R_1=1.5kΩ, R_2=150Ω, C_{L1}= C_{L2}=10pF
	t_{PHL12}		40.8	62	ns	See Figure 6.7, R_1=1.5kΩ, R_2=150Ω, C_{L1}= C_{L2}=10pF
	t_{PLH21}		65.1	98	ns	See Figure 6.7, R_1=1.5kΩ, R_2=150Ω, C_{L1}= C_{L2}=10pF
	t_{PHL21}		49.9	75	ns	See Figure 6.7, R_1=1.5kΩ, R_2=150Ω, C_{L1}= C_{L2}=10pF
Pulse Width Distortion	PWD_{12}		1.9	53	ns	$\lvert t_{PHL12} - t_{PLH12} \rvert$
	PWD_{21}		16.1	53	ns	$\lvert t_{PHL21} - t_{PLH21} \rvert$
Falling Time	t_{f1}		9.26	17	ns	R_1=1.5kΩ, R_2=150Ω, C_{L1}=40pF, C_{L2}=400pF, 0.7*VDD_1 to 0.3*VDD_1
			15.6	27		R_1=1.5kΩ, R_2=150Ω, C_{L1}=40pF, C_{L2}=400pF, 0.9*VDD_1 to 900mV
	t_{f2}		9.6	15	ns	R_1=1.5kΩ, R_2=150Ω, C_{L1}=40pF, C_{L2}=400pF, 0.7*VDD_2 to 0.3*VDD_2
			20.2	31		R_1=1.5kΩ, R_2=150Ω, C_{L1}=40pF, C_{L2}=400pF, 0.9*VDD_1 to 400mV

(VDD_1=2.5V± 10%, VDD_2=2.5V± 10%, T_A=-40℃ to 125℃. Unless otherwise noted, Typical values are at VDD_1= VDD_2= 2.5V, T_A = 25℃)

PARAMETER	*SYMBOL*	*MIN*	*TYP*	*MAX*	*UNIT*	*COMMENT*
Supply current	I_{DD1}(Q0)		5.3	6.5	mA	All Input 0V
	I_{DD2}(Q0)		4.2	5.1	mA	
	I_{DD1}(Q1)		2.8	3.7	mA	All Input at supply
	I_{DD2}(Q1)		1.7	2.5	mA	
	I_{DD1}(2M)		3.75	4.7	mA	All Input with 2MHz, C_{L1}= C_{L2}=10pF
	I_{DD2}(2M)		3.1	3.9	mA	
Data Rate	DR			2	MHz	
Propagation Delay	t_{PLH12}		38.5	58	ns	See Figure 6.7, R_1=1.5kΩ, R_2=150Ω, C_{L1}= C_{L2}=10pF
	t_{PHL12}		45.6	68	ns	See Figure 6.7, R_1=1.5kΩ, R_2=150Ω, C_{L1}= C_{L2}=10pF

	t_{PLH21}		65.4	98	ns	See Figure 6.7, R_1=1.5kΩ, R_2=150Ω, C_{L1}= C_{L2}=10pF
	t_{PHL21}		71.4	107	ns	See Figure 6.7, R_1=1.5kΩ, R_2=150Ω, C_{L1}= C_{L2}=10pF
Pulse Width Distortion	PWD_{12}		7.2	53	ns	$\lvert t_{PHL12} - t_{PLH12} \rvert$
	PWD_{21}		6.1	53	ns	$\lvert t_{PHL21} - t_{PLH21} \rvert$
Falling Time	t_{f1}		21.4	34	ns	R_1=1.5kΩ, R_2=150Ω, C_{L1}=40pF, C_{L2}=400pF, 0.9*VDD_1 to 900mV
	t_{f2}		11.6	18	ns	R_1=1.5kΩ, R_2=150Ω, C_{L1}=40pF, C_{L2}=400pF, 0.7*VDD_2 to 0.3*VDD_2
			21.8	33		R_1=1.5kΩ, R_2=150Ω, C_{L1}=40pF, C_{L2}=400pF, 0.9*VDD_1 to 400mV

6.2. Typical Performance Characteristics

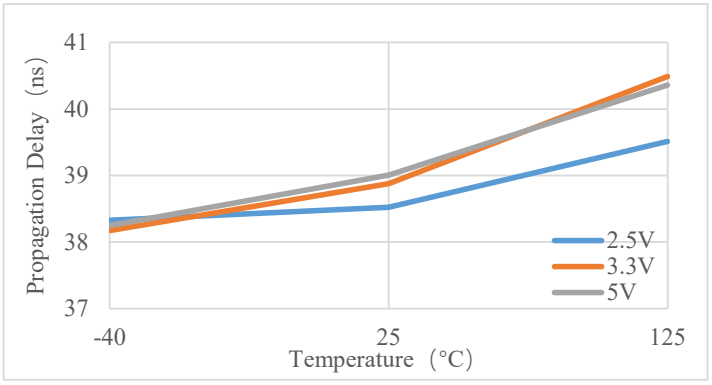


Figure 6. 1 t_{PLH12} Rising Edge Propagation Delay Vs Temperature

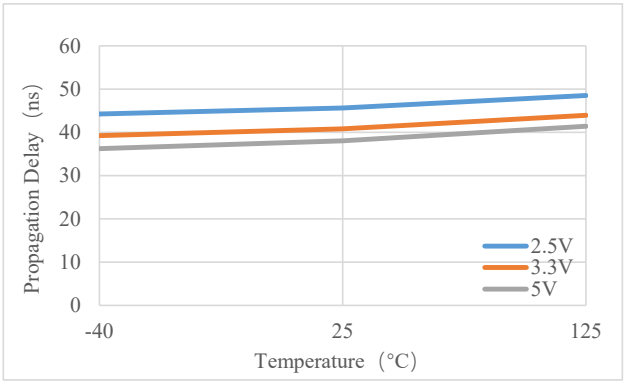


Figure 6. 2 t_{PHL12} Falling Edge Propagation Delay Vs Temperature

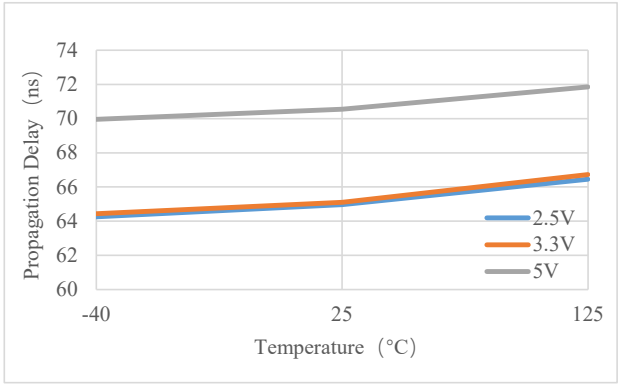


Figure 6. 3 t_{PLH21} Rising Edge Propagation Delay Vs Temperature

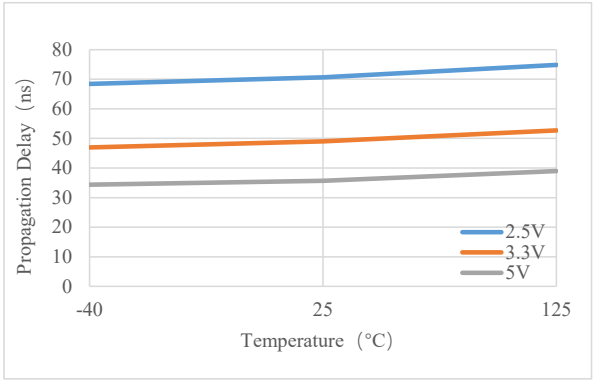


Figure 6. 4 t_{PHL21} Falling Edge Propagation Delay Vs Temperature

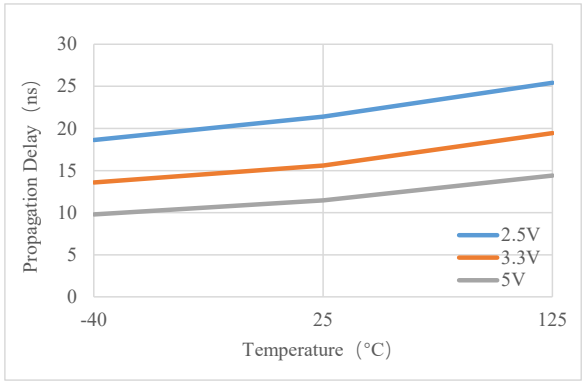


Figure 6. 5 t_{f1} (0.9*VDD_1 to 900mV) Falling time(@40pF) Vs Temperature

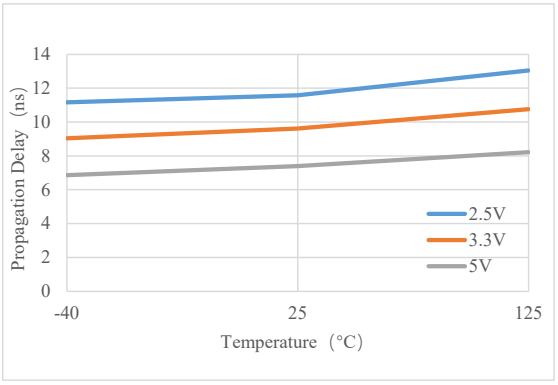


Figure 6. 6 t_{f2} (0.7*VDD_2 to 0.3*VDD_2) Falling time(@400pF) Vs Temperature

6.3. Parameter Measurement Information

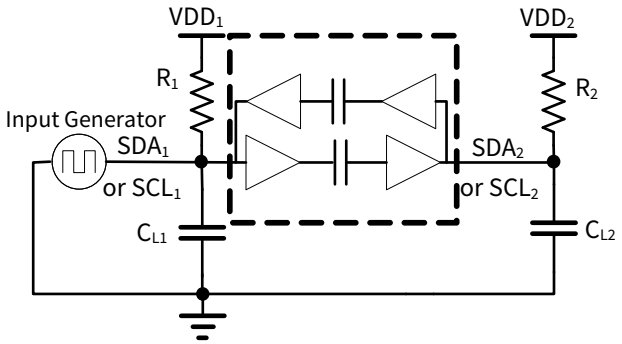


Figure 6. 7 Switching Characteristic Test Circuit

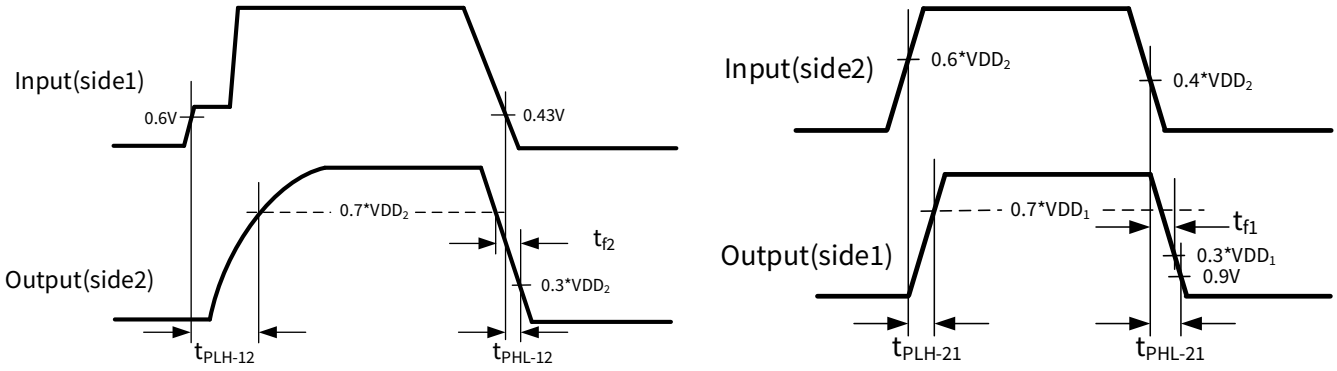


Figure 6. 8 Timing Diagram

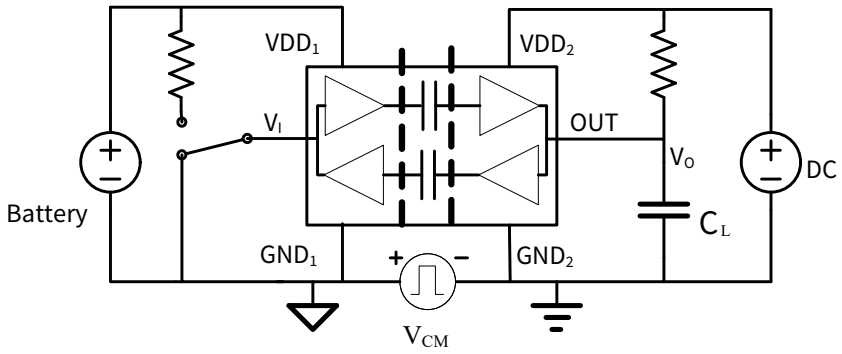


Figure 6. 9 Common-Mode Transient Immunity Test Circuit

7. High Voltage Feature Description

7.1. Insulation and Safety Related Specifications

Parameters	*Symbol*	*Value*			*Unit*	*Comments*
		SOP8	*SOW16*	*SOWW8*		
Minimum External Clearance	CLR	4	8	15	mm	IEC 60664-1:2007
Minimum External Creepage	CPG	4	8	15	mm	IEC 60664-1:2007
Distance Through Insulation	DTI	28			μm	Distance through insulation
Tracking Resistance (Comparative Tracking Index)	CTI	>600			V	DIN EN 60112 (VDE 0303-11); IEC 60112
Material Group		I				IEC 60664-1

Description	*Test Condition*	*Value*		
		SOP8	SOW16	SOWW8
Overvoltage Category per IEC60664-1	For Rated Mains Voltage ≤ 150V_{rms}	I to IV	I to IV	I to IV
	For Rated Mains Voltage ≤ 300V_{rms}	I to IV	I to IV	I to IV
	For Rated Mains Voltage ≤ 600V_{rms}	I to IV	I to IV	I to IV
	For Rated Mains Voltage ≤ 1000V_{rms}	I to III	I to III	I to III
Climatic Classification		40/125/21		
Pollution Degree per DIN VDE 0110,		2		

7.2. Insulation Characteristics

Description	Test Condition	Symbol	Value			Unit
			SOP8	SOW16	SOWW8	
Maximum repetitive isolation voltage		V_{IORM}	565	2121	2121	V_{PEAK}
Maximum working isolation voltage	AC Voltage	V_{IOWM}	400	1500	1500	V_{RMS}
	DC Voltage		565	2121	2121	V_{DC}
Apparent Charge	Method a, after Input/output safety test subgroup 2/3, Vini=V_{IOTM}, t_{ini} = 60 s, $V_{pd(m)}$=1.2*V_{IORM}, t_m=10s.	q_{pd}		<5	<5	pC
	Method a, after environmental tests subgroup 1, Vini=V_{IOTM}, t_{ini}=60s ,$V_{pd(m)}$=1.6*V_{IORM}, t_m=10s					pC
	Method b, routine test (100% production) and preconditioning (type test); V_{ini}=1.2*V_{IOTM}, t_{ini}=1s $V_{pd(m)}$=1.875*V_{IORM}, t_m=1s （method b1） or $V_{pd(m)}$=Vini, t_m=t_{ini}(method b2)					pC
Apparent Charge	Method a, after Input/output safety test subgroup 2/3, Vini=V_{IOTM}, t_{ini} = 60 s, $V_{pd(m)}$=1.2*V_{IORM}, t_m=10s.	q_{pd}	<5			pC
	Method a, after environmental tests subgroup 1, Vini=V_{IOTM}, t_{ini}=60s, $V_{pd(m)}$=1.3*V_{IORM}, t_m=10s					pC
	Method b, routine test (100% production) and preconditioning (type test); V_{ini}=1.2*V_{IOTM}, t_{ini}=1s $V_{pd(m)}$=1.5*V_{IORM}, t_m=1s （method b1） or $V_{pd(m)}$=Vini, t_m=t_{ini}(method b2)					pC
Maximum transient isolation voltage	t = 60 sec	V_{IOTM}	5300	8000	12000	V_{PEAK}
Maximum impulse voltage	Tested in air, 1.2/50μs waveform per IEC62368-1	V_{IMP}	5384	7700	7700	V_{PEAK}

Description	Test Condition	Symbol	Value			Unit
			SOP8	SOW16	SOWW8	
Maximum Surge Isolation Voltage	Test method per IEC62368-1, 1.2/50μs waveform, $V_{IOSM} \geqslant V_{IMP} \times 1.3$	V_{IOSM}	7000	10000	10000	V_{PEAK}
Isolation resistance	V_{IO} =500V, T_{amb}=25℃	R_{IO}	>10^{12}	>10^{12}	>10^{12}	Ω
	V_{IO} =500V, 100℃ ≤ T_{amb} ≤ 125℃	R_{IO}	>10^{11}	>10^{11}	>10^{11}	Ω
	V_{IO} =500V, T_{amb}=T_s	R_{IO}	>10^{9}	>10^{9}	>10^{9}	Ω
Isolation capacitance	f = 1MHz	C_{IO}	0.8	0.8	0.8	pF
Safety total power dissipation	V_I = 5.5V, T_J = 150 ℃, T_A = 25 ℃	Ps	908	1445	1584	mW
Safety input, output, or supply current	θ_{JA} = 137.7℃/W for SOP8, V_I = 5.5V, T_J = 150 ℃, T_A = 25 ℃	Is	165	/	/	mA
	θ_{JA} = 86℃/W for SOW16, V_I = 5.5V, T_J = 150 ℃, T_A = 25 ℃		/	262.7	/	mA
	θ_{JA} = 78.9℃/W for SOWW8, V_I = 5.5V, T_J = 150 ℃, T_A = 25 ℃		/	/	288	mA
Maximum safety temperature		Ts	150	150	150	℃
UL1577						
Insulation voltage per UL	$V_{TEST} = V_{ISO}$, t = 60 s (qualification), $V_{TEST} = 1.2 \times V_{ISO}$, t = 1 s (100% production test)	V_{ISO}	3750	5000	8000	V_{RMS}

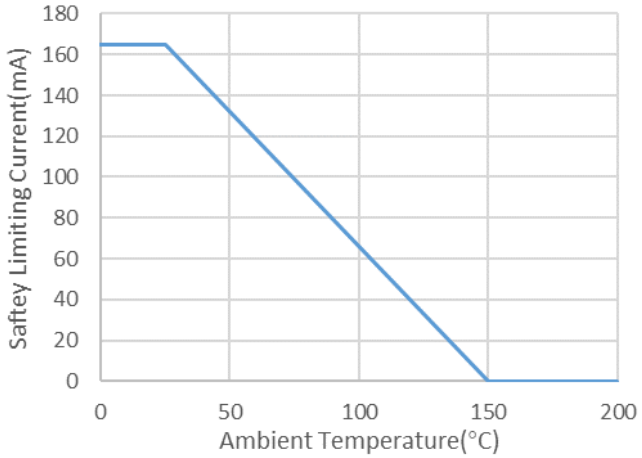


Figure 7.1 NSI8200-DSPR Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN VDE V 0884-17

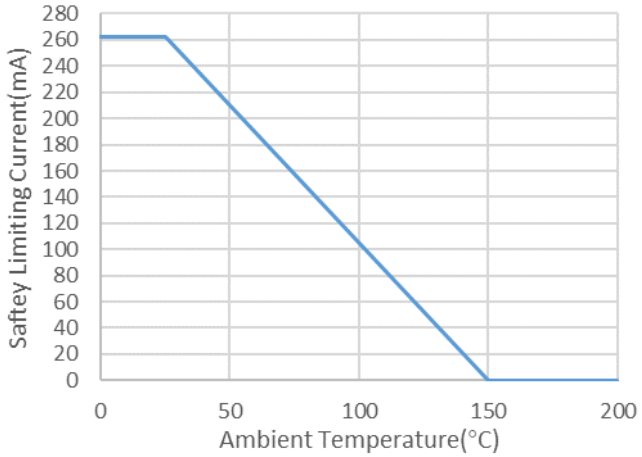


Figure 7.2 NSI8200-DSWR Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN VDE V 0884-17

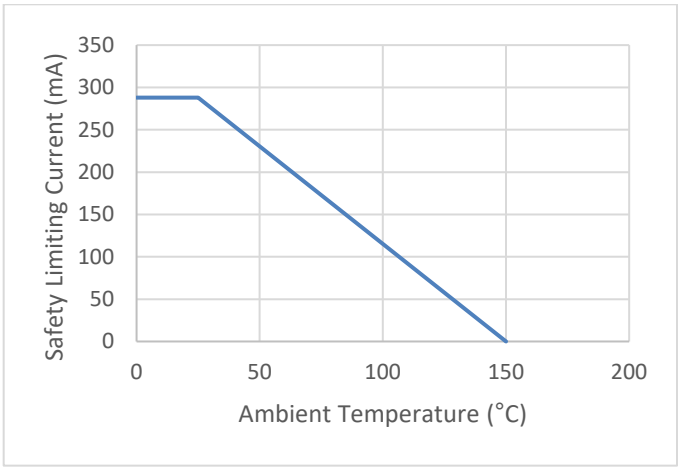


Figure 7.3 NSI8200-DSWWAR Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN VDE V 0884-17

7.3. Regulatory Information

The NSI8200-DSPR are approved by the organizations listed in table.

CUL		*VDE*	*CQC*
UL 1577 Component Recognition Program	Approved under CSA Component Acceptance Notice 5A	DIN VDE V 0884-17	Certified according to GB4943.1
Single Protection, 3750V_{RMS} Isolation voltage	Single Protection, 3750V_{RMS} Isolation voltage	Basic Insulation V_{IORM}=565Vpeak V_{IOTM}=5300Vpeak V_{IOSM}=7000Vpeak	Basic insulation
File (E500602)	File (E500602)	File (pending)	File (pending)

The NSI8200-DSWR are approved by the organizations listed in table.

CUL		*VDE*	*CQC*
UL 1577 Component Recognition Program	Approved under CSA Component Acceptance Notice 5A	DIN VDE V 0884-17	Certified according to GB4943.1
Single Protection, 5000V_{RMS} Isolation voltage	Single Protection, 5000V_{RMS} Isolation voltage	Reinforced V_{IORM}=2121Vpeak V_{IOTM}=8000Vpeak V_{IOSM}=10000Vpeak	Reinforced insulation
File (E500602)	File (E500602)	File (pending)	File (CQC20001264939)

The NSI8200-DSWWAR are approved by the organizations listed in table.

CUL		*VDE*	*CQC*
UL 1577 Component Recognition Program	Approved under CSA Component Acceptance Notice 5A	DIN VDE V 0884-17	Certified according to GB4943.1
Single Protection, 8000V_{RMS} Isolation voltage	Single Protection, 8000V_{RMS} Isolation voltage	Reinforced V_{IORM}=2121Vpeak V_{IOTM}=12000Vpeak V_{IOSM}=10000Vpeak	Reinforced insulation
File (pending)	File (pending)	File (pending)	File (pending)

8. Function Description

8.1. Overview

The NSI8200 is a bidirectional isolator based on a capacitive isolation barrier technique. The NSI8200 devices are compatible with I^2C interface. Internally, the I^2C interface is split into two unidirectional channels communicating in opposing directions via a dedicate capacitive isolation channel for each. The digital signal is modulated with RF carrier generated by the internal oscillator at the transmitter side. Then it is transferred through the capacitive isolation barrier and demodulated at the receiver side.

The NSI8200 devices are high reliability dual-channel bidirectional isolators for clock and data lines. The NSI8200 is suitable for multi-master application.

The Side 2 logic levels of NSI8200 are standard I^2C value, and the maximum load for side 2 is ≤ 400pF. So multiple NSI8200 devices connected to a bus by their Side 2 pins can communicate with each other and with other I^2C compatible devices.

The Side 1 logic levels of NSI8200 are not standard I^2C value. The low-level output voltage V_{OL} is greater than the high-level input voltage V_{IH}, as shown in Figure 8. 1. This prevents an output logic low at Side 1 being transmitted back to Side 2 and pulling down the I^2C bus.

The NSI8200 device is safety certified by UL1577 support several withstand isolation voltages (3.75kV$_{RMS}$, 5kV$_{RMS}$), while providing high electromagnetic immunity and low emissions at low power consumption. The I^2C clock frequency of the NSI8200 is up to 2MHz. Wide supply voltage of the NSI8200 device support to connect with most digital interface directly, easy to do the level shifting. High system level EMC performance enhance reliability and stability of use.

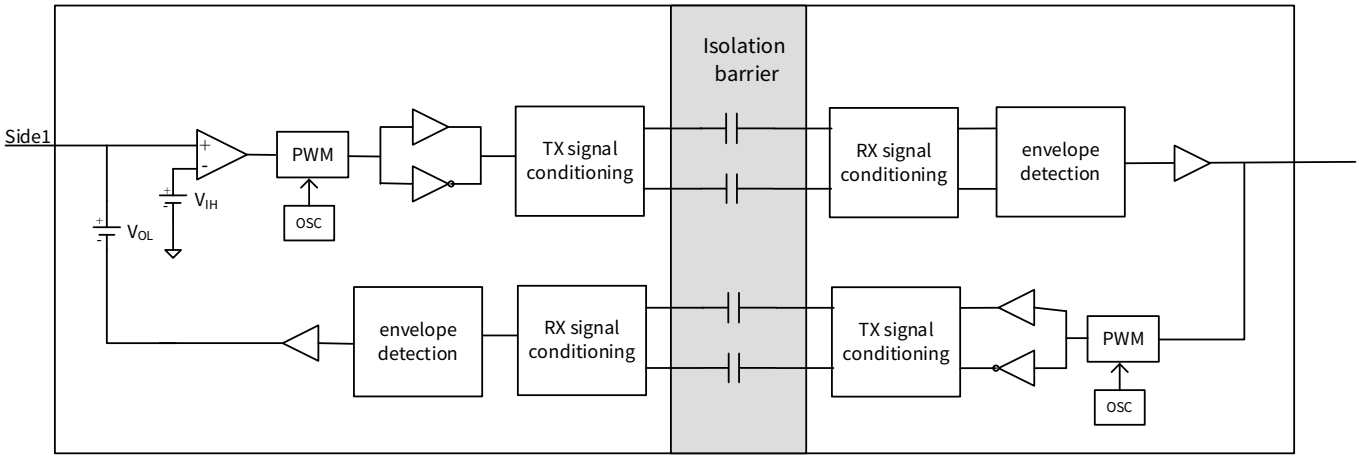


Figure 8. 1 Simplified Channel Diagram

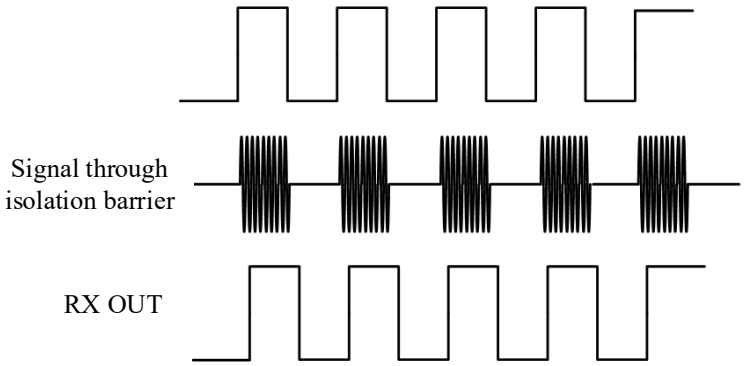


Figure 8. 2 OOK Based Modulation Scheme

8.2. Protection Features

In order to deal with the strong short current caused by the pull-up resistance being short circuited or the resistance value being lower than 5 ohms, the I2C bus pins on side 2 include a short circuit protection circuit to protect the bus pins (SDA2 and SCL2).

Thermal shutdown is integrated in the NSI8200 to protect the device from high current events. If the junction temperature of the device exceeds the thermal shutdown threshold of 175℃ (typical), the device will shut down, disabling the I2C circuits and releasing the I2C bus. In addition, the shutdown condition is cleared when the junction temperature drops the thermal shutdown hysteresis temperature below the thermal shutdown temperature of the device.

8.3. Functional Modes

The Table 8. 1 shows the functional of NSI8200.The NSI8200 is high impedance output when VDDIN is unready and VDDOUT is ready as shown in.

Table 8. 1 Output Status vs Power Status

INPUT	*VDD_1 STATUS*	*VDD_2 STATUS*	*OUTPUT*	*COMMENT*
H	Ready	Ready	Z	Normal operation.
L	Ready	Ready	L	
X	Unready	Ready	Z	The output follows the same status with the input within 60μs after input side VDD1 is powered on.
X	Ready	Unready	Undetermined	The output follows the same status with the input within 60μs after output side VDD2 is powered on.

1. H = High Level; L = Low Level; Z = High Impedance or Float; X = Irrelevant.

9. Application Note

9.1. PCB Layout

The NSI8200 requires a 0.1 μF bypass capacitor between VDD_1 and GND_1, VDD_2 and GND_2. The capacitor should be placed as close as possible to the package. Figure 9.1 to Figure 9.4 show the recommended PCB layout, make sure the space under the chip should keep free from planes, traces, pads and via. The pull-up resistors required for both Side 1 and Side 2 buses. And the value of the resistors depends on the number of I^2C devices on the bus.

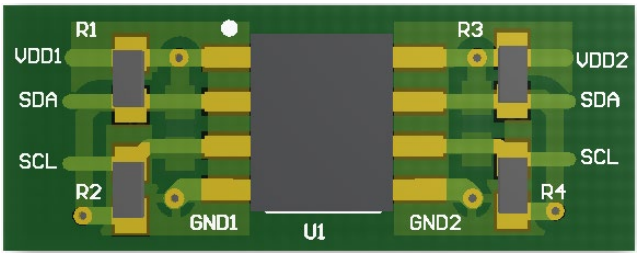


Figure 9.1 NSI8200-DSPR Recommended PCB Layout —Top Layer

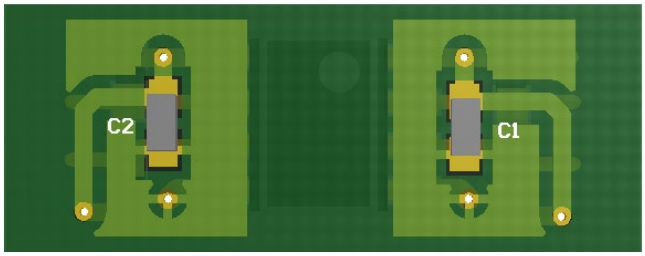


Figure 9.2 NSI8200-DSPR Recommended PCB Layout —Bottom Layer

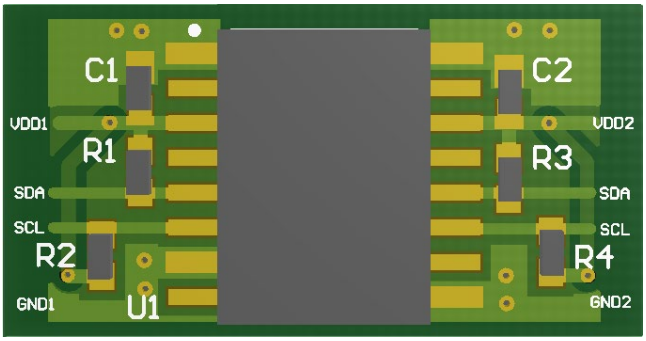


Figure 9.3 NSI8200-DSWR Recommended PCB Layout —Top Layer

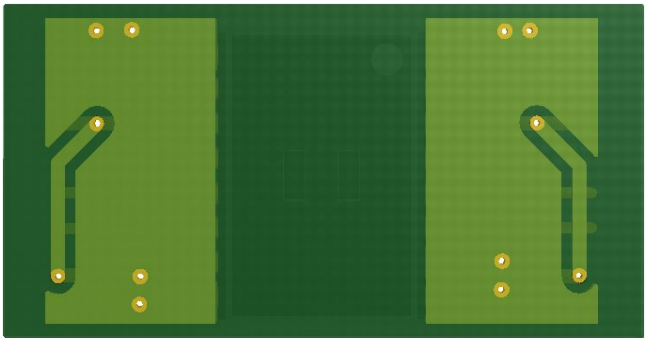
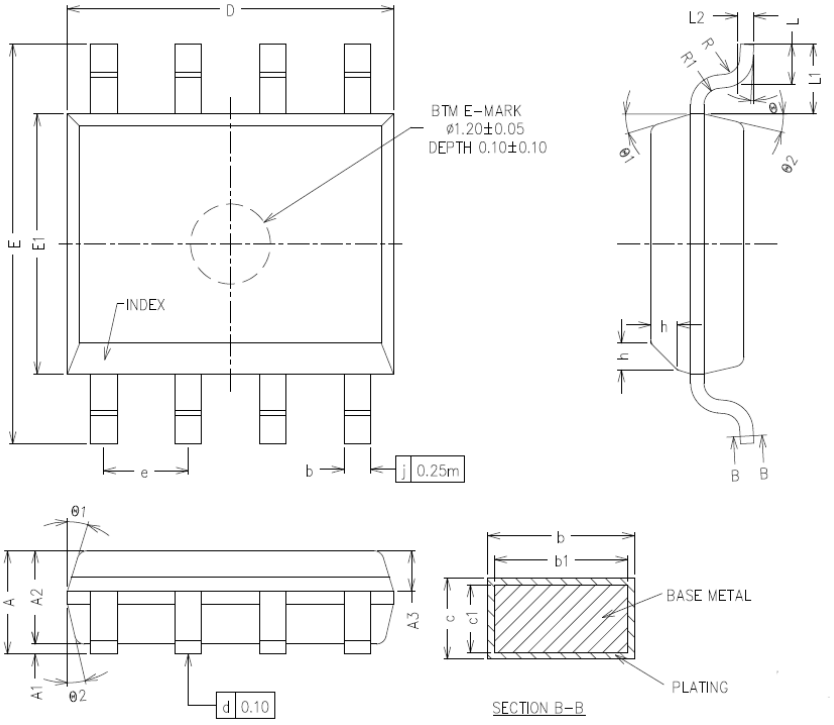


Figure 9.4 NSI8200-DSWR Recommended PCB Layout —Bottom Layer

10. Package Information

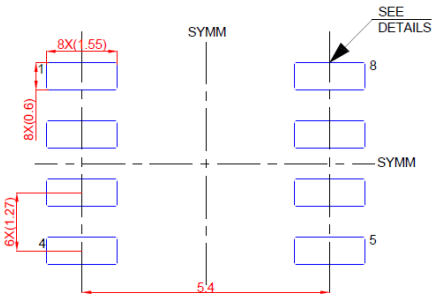


COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

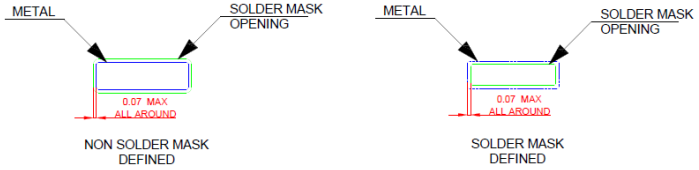
SYMBOL	MIN	NOM	MAX
A	1.35	1.55	1.75
A1	0.10	–	0.25
A2	1.30	1.40	1.50
A3	0.50	0.60	0.70
b	0.38	–	0.47
b1	0.37	0.40	0.43
c	0.17	–	0.25
c1	0.17	0.20	0.23
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.17	1.27	1.37
L	0.45	0.60	0.80
L1	1.04REF		
L2	0.25BSC		
R	0.07	–	–
R1	0.07	–	–
h	0.30	0.40	0.50
θ	0°	–	8°
θ1	15°	17°	19°
θ2	11°	13°	15°

NOTE: This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.

Figure 10.1 SOP8 Package Shape and Dimension in millimeters

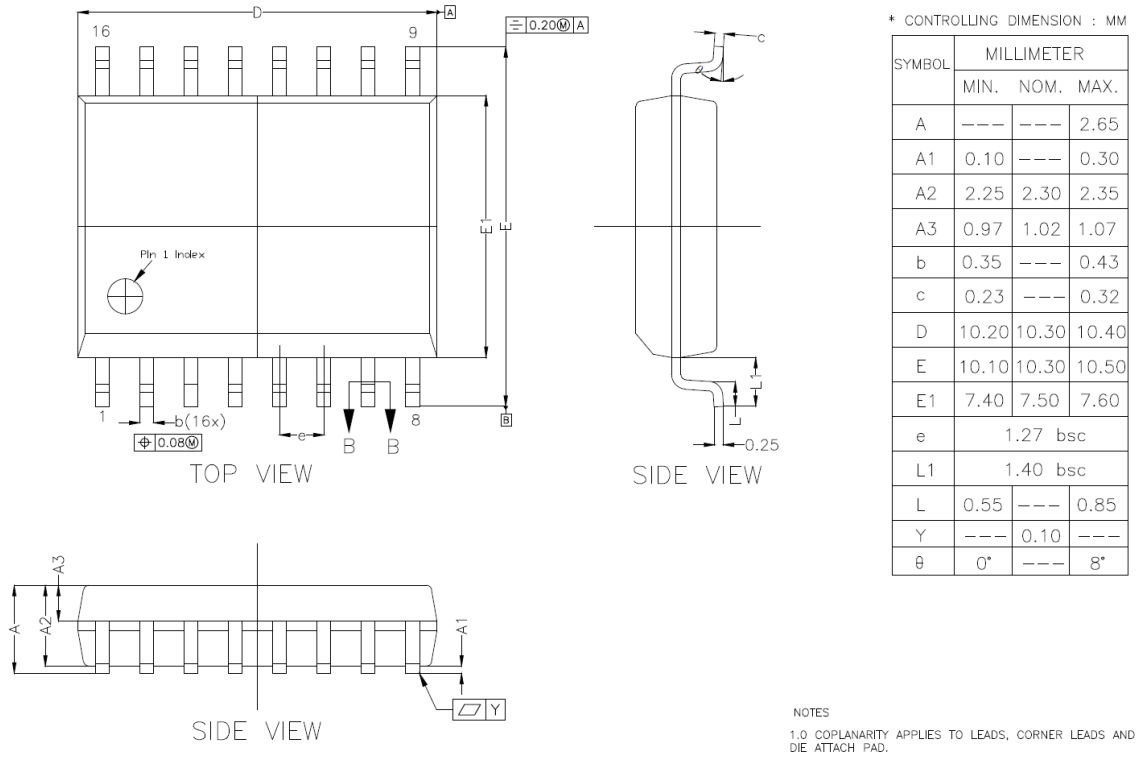


LAND PATTERN EXAMPLE(mm)



SOLDER MASK DETAILS

Figure 10.2 SOP8 Package Board Layout Example



* CONTROLLING DIMENSION : MM

SYMBOL	MILLIMETER		
	MIN.	NOM.	MAX.
A	---	---	2.65
A1	0.10	---	0.30
A2	2.25	2.30	2.35
A3	0.97	1.02	1.07
b	0.35	---	0.43
c	0.23	---	0.32
D	10.20	10.30	10.40
E	10.10	10.30	10.50
E1	7.40	7.50	7.60
e	1.27 bsc		
L1	1.40 bsc		
L	0.55	---	0.85
Y	---	0.10	---
θ	0°	---	8°

NOTE : This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.

Figure 10.3 SOW16 Package Shape and Dimension in millimeters

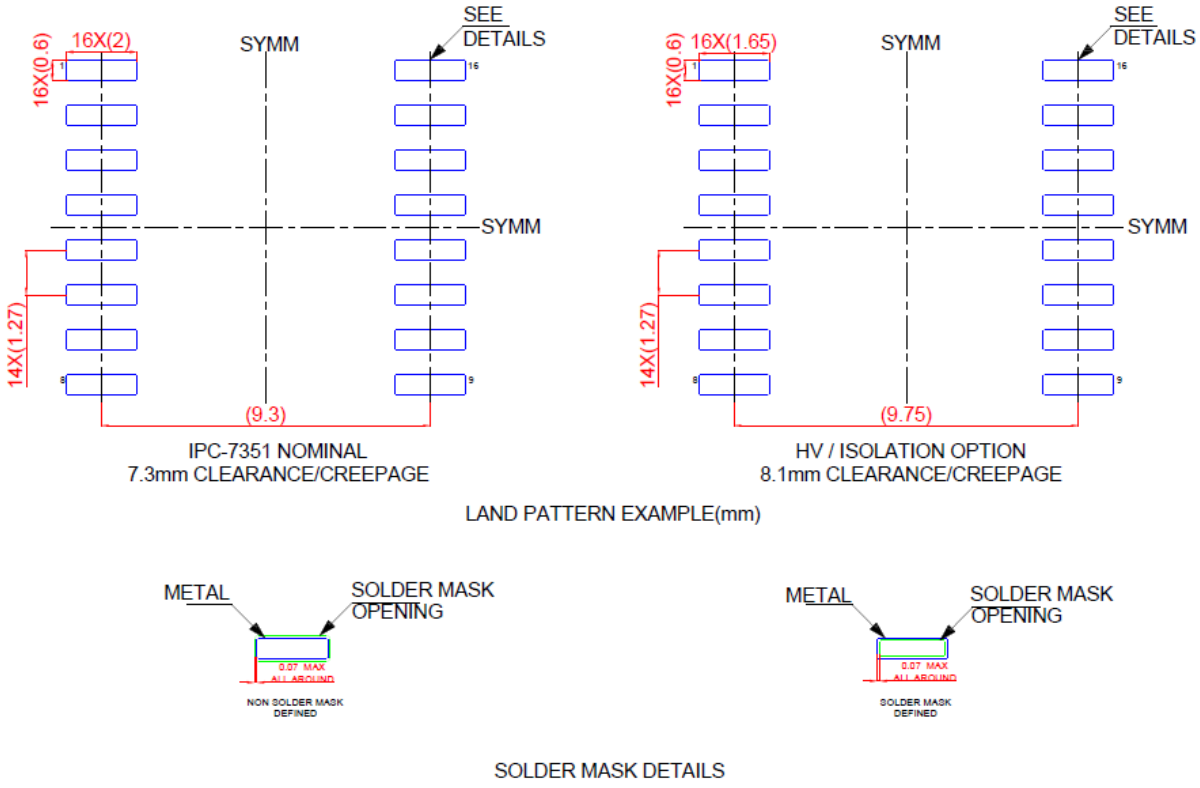
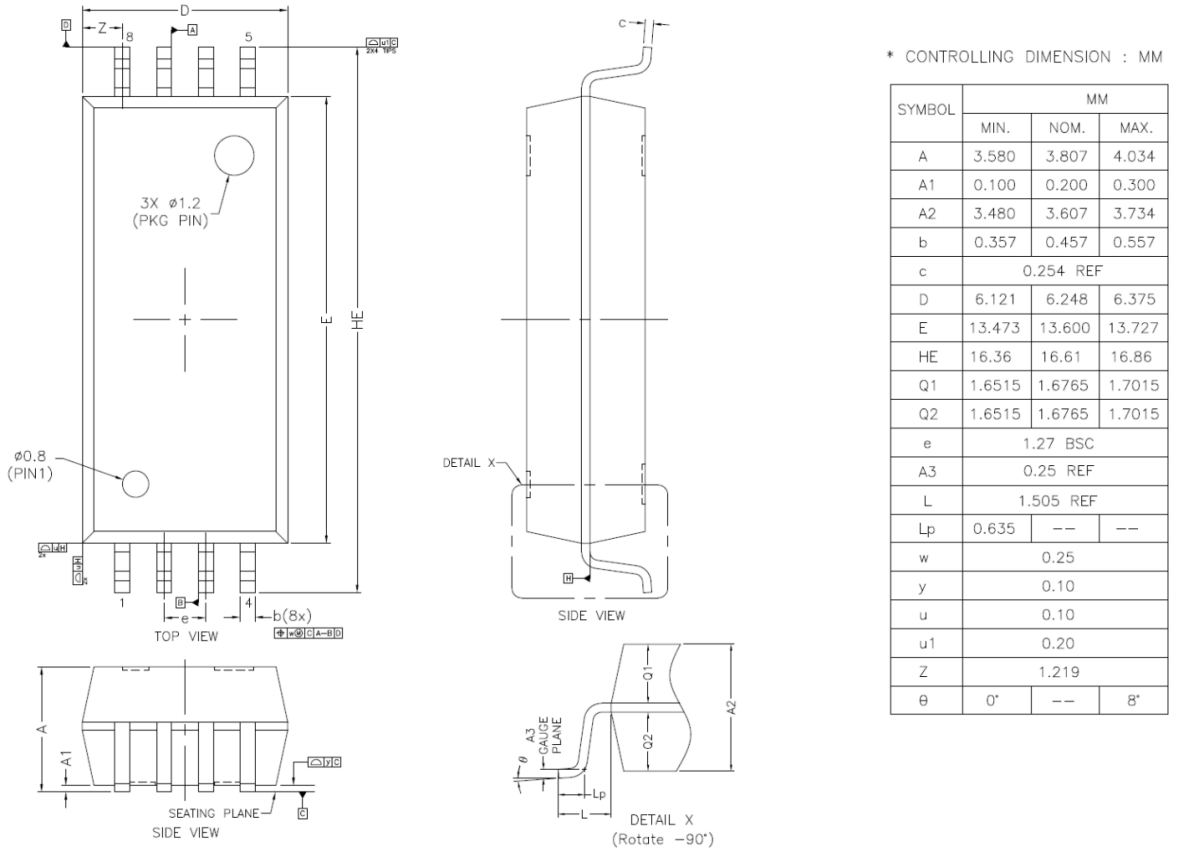


Figure 10.4 SOW16 Package Board Layout Example



* CONTROLLING DIMENSION : MM

SYMBOL	MM		
	MIN.	NOM.	MAX.
A	3.580	3.807	4.034
A1	0.100	0.200	0.300
A2	3.480	3.607	3.734
b	0.357	0.457	0.557
c	0.254 REF		
D	6.121	6.248	6.375
E	13.473	13.600	13.727
HE	16.36	16.61	16.86
Q1	1.6515	1.6765	1.7015
Q2	1.6515	1.6765	1.7015
e	1.27 BSC		
A3	0.25 REF		
L	1.505 REF		
Lp	0.635	--	--
w	0.25		
y	0.10		
u	0.10		
u1	0.20		
Z	1.219		
θ	0°	--	8°

NOTE: This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.

Figure 10.5 SOWW8 Package Shape and Dimension in millimeters

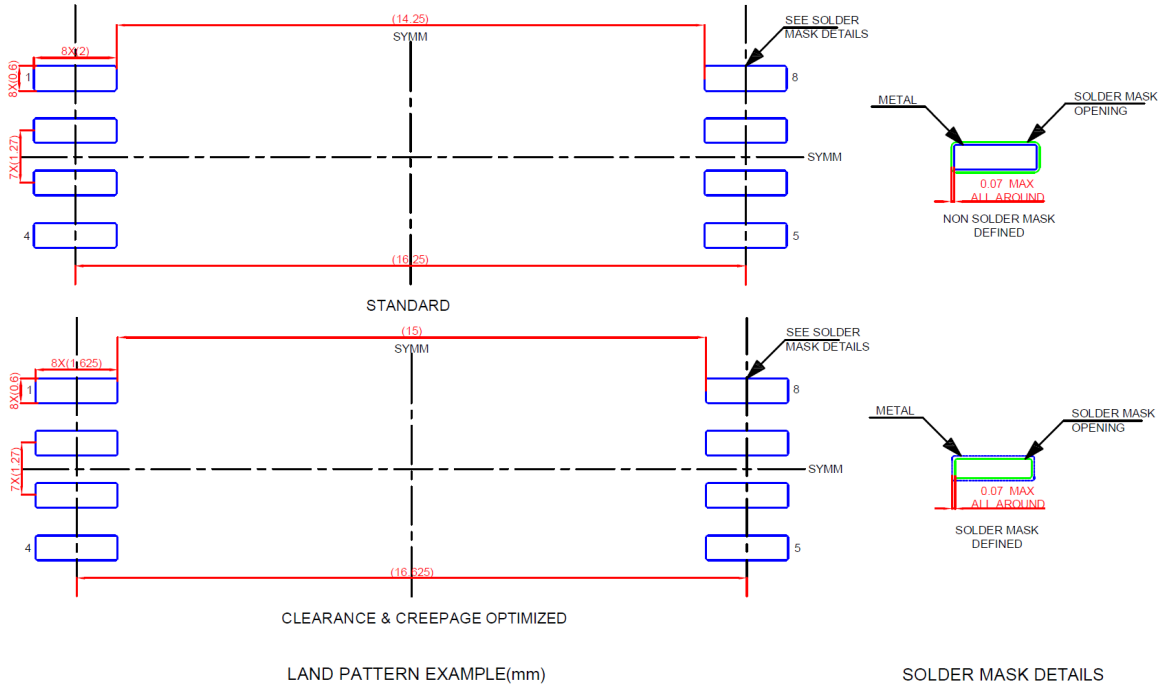
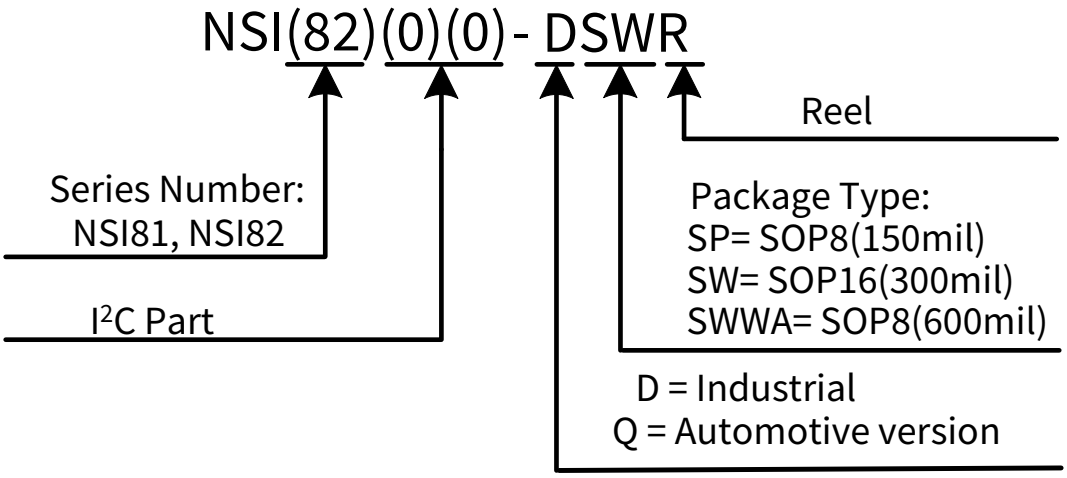


Figure 10.6 SOWW8 Package Board Layout Example

11. Order Information

Part No.	*Isolation Rating(kV)*	*Number of Side 1 Inputs*	*Number of Side 2 Inputs*	*Max Data Rate (MHz)*	*Operating Temperature*	*MSL*	***Package Type***	***Package Drawing***	*SPQ*
NSI8200-DSPR	3.75	2	2	2	-40 to 125℃	1	SOP8	SOP8	2500
NSI8200-DSWR	5	2	2	2	-40 to 125℃	2	SOP16(300mil)	SOW16	1000
NSI8200-DSWWAR	8	2	2	2	-40 to 125℃	3	SOP8(600mil)	SOWW8	1000
NOTE: All packages are RoHS-compliant with peak reflow temperatures of 260 ℃ according to the JEDEC industry standard classifications and peak solder temperatures.									

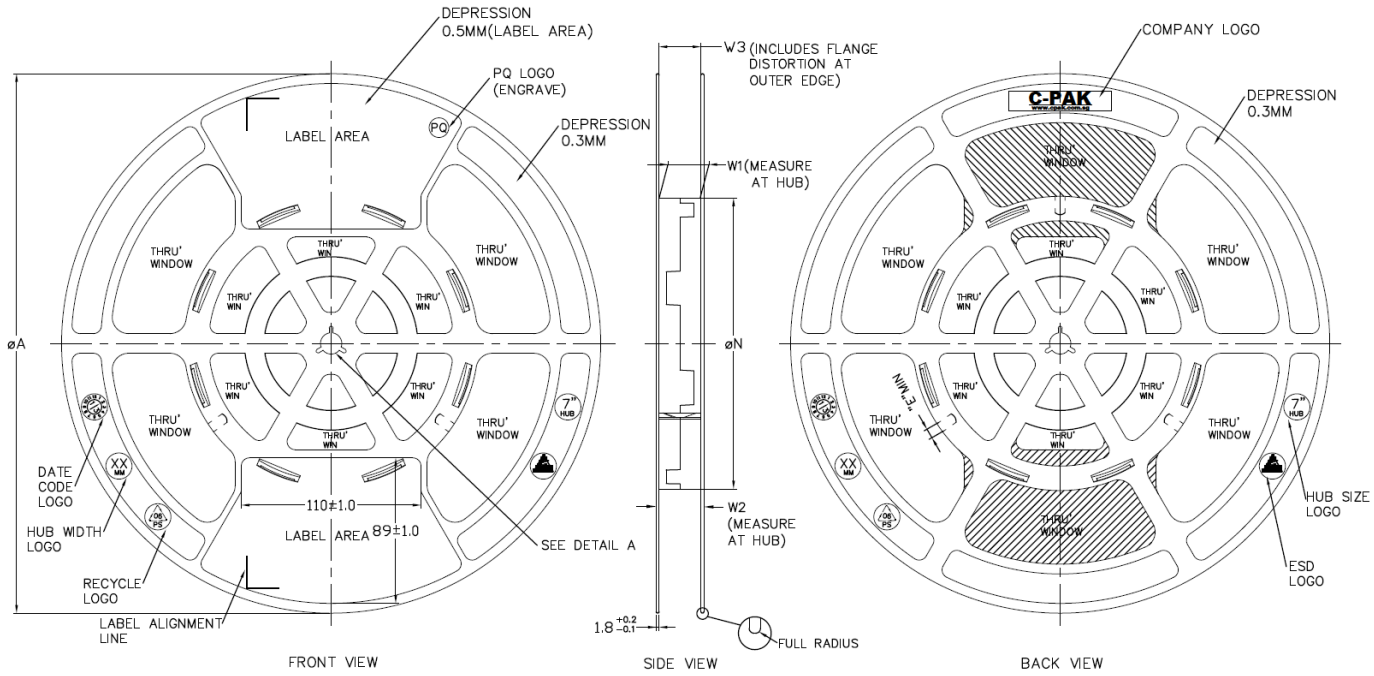
Part Number Rule:

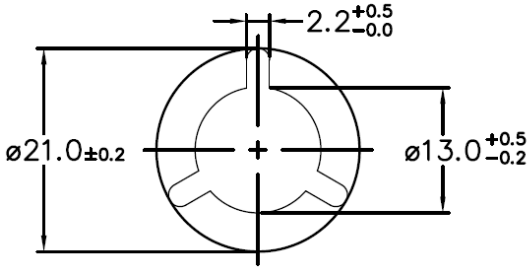


12. Documentation Support

Part Number	***Product Folder***	***Datasheet***	***Technical Documents***	***Isolator selection guide***
NSI8200-DSPR	Click here	Click here	Click here	Click here
NSI8200-DSWR	Click here	Click here	Click here	Click here
NSI8200-DSWWAR	Click here	Click here	Click here	Click here

13. Tape and Reel Information

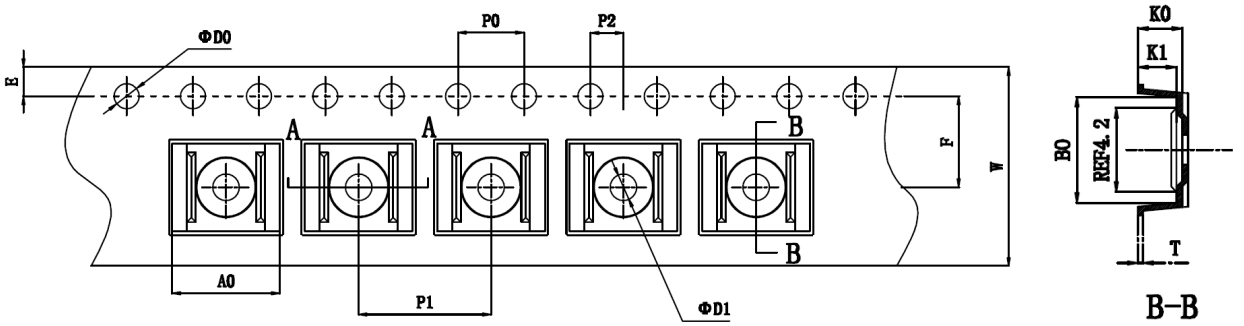


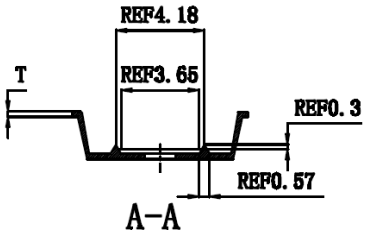


ARBOR HOLE
DETAIL A
SCALE : 3:1

PRODUCT SPECIFICATION						
TAPE WIDTH	øA ±2.0	øN ±2.0	W1	W2 (MAX)	W3	E (MIN)
08MM	330	178	8.4 +1.5 −0.0	14.4	SHALL ACCOMMODATE TAPE WIDTH WITHOUT INTERFERENCE	5.5
12MM	330	178	12.4 +2.0 −0.0	18.4		5.5
16MM	330	178	16.4 +2.0 −0.0	22.4		5.5
24MM	330	178	24.4 +2.0 −0.0	30.4		5.5
32MM	330	178	32.4 +2.0 −0.0	38.4		5.5

SURFACE RESISTIVITY			
LEGEND	SR RANGE	TYPE	COLOUR
A	BELOW 10^{12}	ANTISTATIC	ALL TYPES
B	10^{6} TO 10^{11}	STATIC DISSIPATIVE	BLACK ONLY
C	10^{5} & BELOW 10^{5}	CONDUCTIVE (GENERIC)	BLACK ONLY
E	10^{9} TO 10^{11}	ANTISTATIC (COATED)	ALL TYPES





E	1.75±0.10
F	5.5±0.10
P2	2.00±0.10
D0	1.55±0.05
D1	1.6±0.10
P0	4.00±0.10
10P0	40.00±0.20

W	12.00±0.30
P1	8.00±0.10
A0	6.50±0.10
B0	5.30±0.10
K0	2.20±0.10
K1	1.90±0.10
T	0.30±0.05

NOTES:
1. Cumulative Tolerance of 10 sprocket holes is ±0.20.
2. All dimensions in millimeters unless otherwise stated.
3. Surface resistivity: $10^5 \sim 10^9\ \Omega$

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

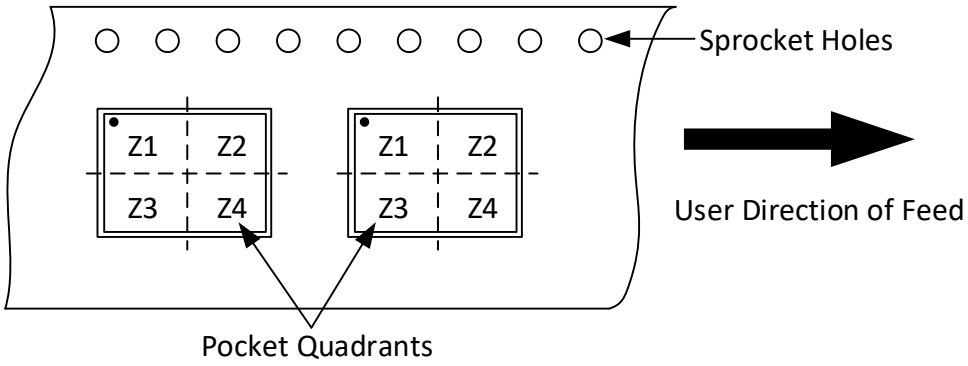
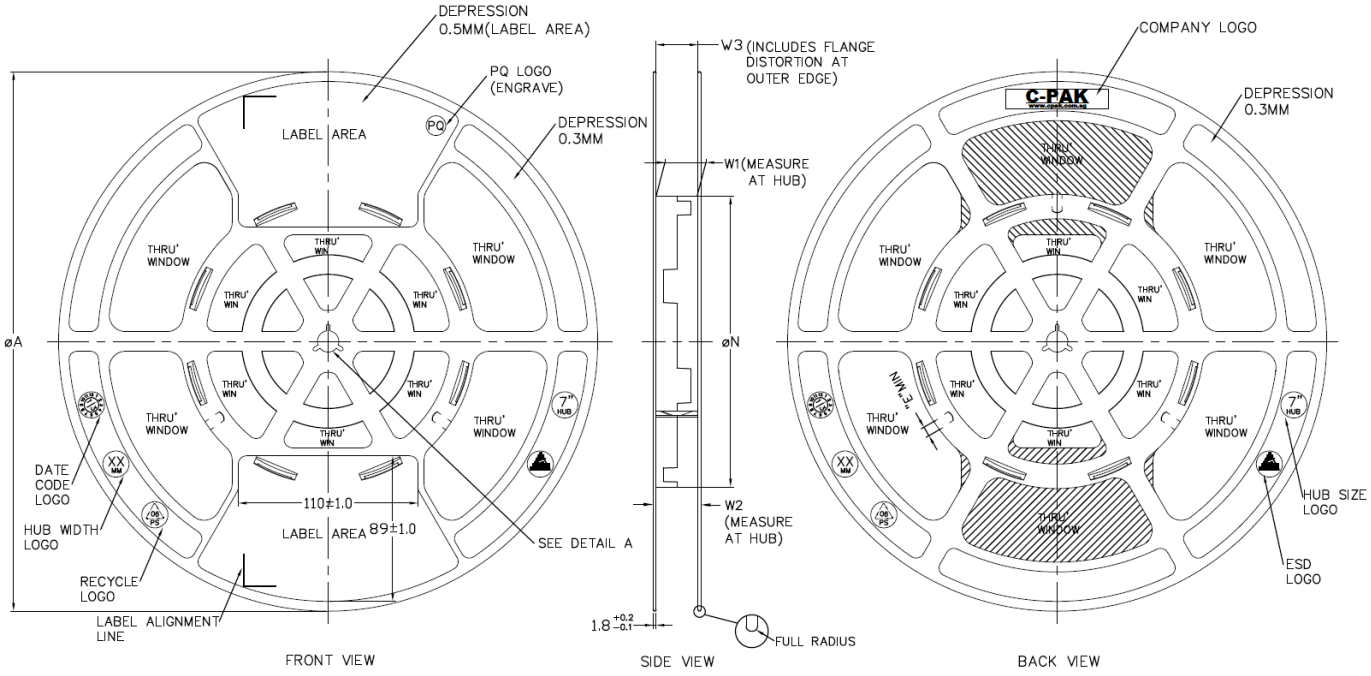
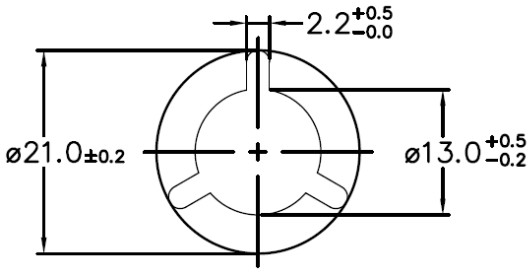


Figure 13. 1 Tape and Reel Information of SOP8

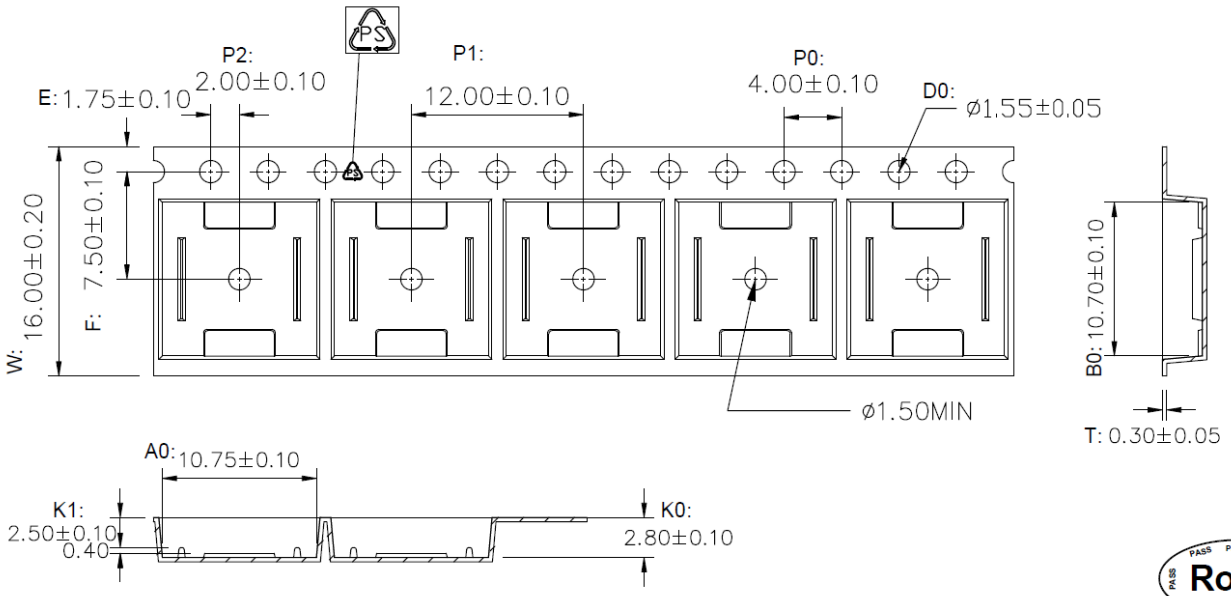




ARBOR HOLE
DETAIL A
SCALE : 3:1

PRODUCT SPECIFICATION						
TAPE WIDTH	øA ±2.0	øN ±2.0	W1	W2 (MAX)	W3	E (MIN)
08MM	330	178	8.4 +1.5 −0.0	14.4	SHALL ACCOMMODATE TAPE WIDTH WITHOUT INTERFERENCE	5.5
12MM	330	178	12.4 +2.0 −0.0	18.4		5.5
16MM	330	178	16.4 +2.0 −0.0	22.4		5.5
24MM	330	178	24.4 +2.0 −0.0	30.4		5.5
32MM	330	178	32.4 +2.0 −0.0	38.4		5.5

SURFACE RESISTIVITY			
LEGEND	SR RANGE	TYPE	COLOUR
A	BELOW 10^{12}	ANTISTATIC	ALL TYPES
B	10^{8} TO 10^{11}	STATIC DISSIPATIVE	BLACK ONLY
C	10^{5} & BELOW 10^{5}	CONDUCTIVE (GENERIC)	BLACK ONLY
E	10^{9} TO 10^{11}	ANTISTATIC (COATED)	ALL TYPES



1. 10 sprocket hole pitch cumulative tolerance ±0.20 .
2. Carrier camber is within 1 mm in 250 mm.
3. Material : Black Conductive Polystyrene Alloy .
4. All dimensions meet EIA-481 requirements.
5. Thickness : 0.30±0.05mm.
6. Packing length per 22" reel : 378 Meters.
7. Component load per 13" reel : 1000 pcs.
8. Surface resistivity : 10^{5} ~ 10^{10} Ω

W	16.00±0.20
A0	10.75±0.10
B0	10.70±0.10
K0	2.80±0.10
K1	2.50±0.10

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

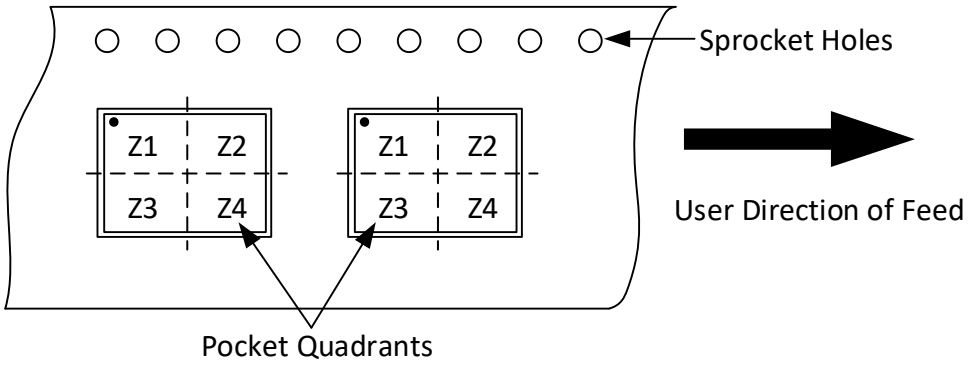
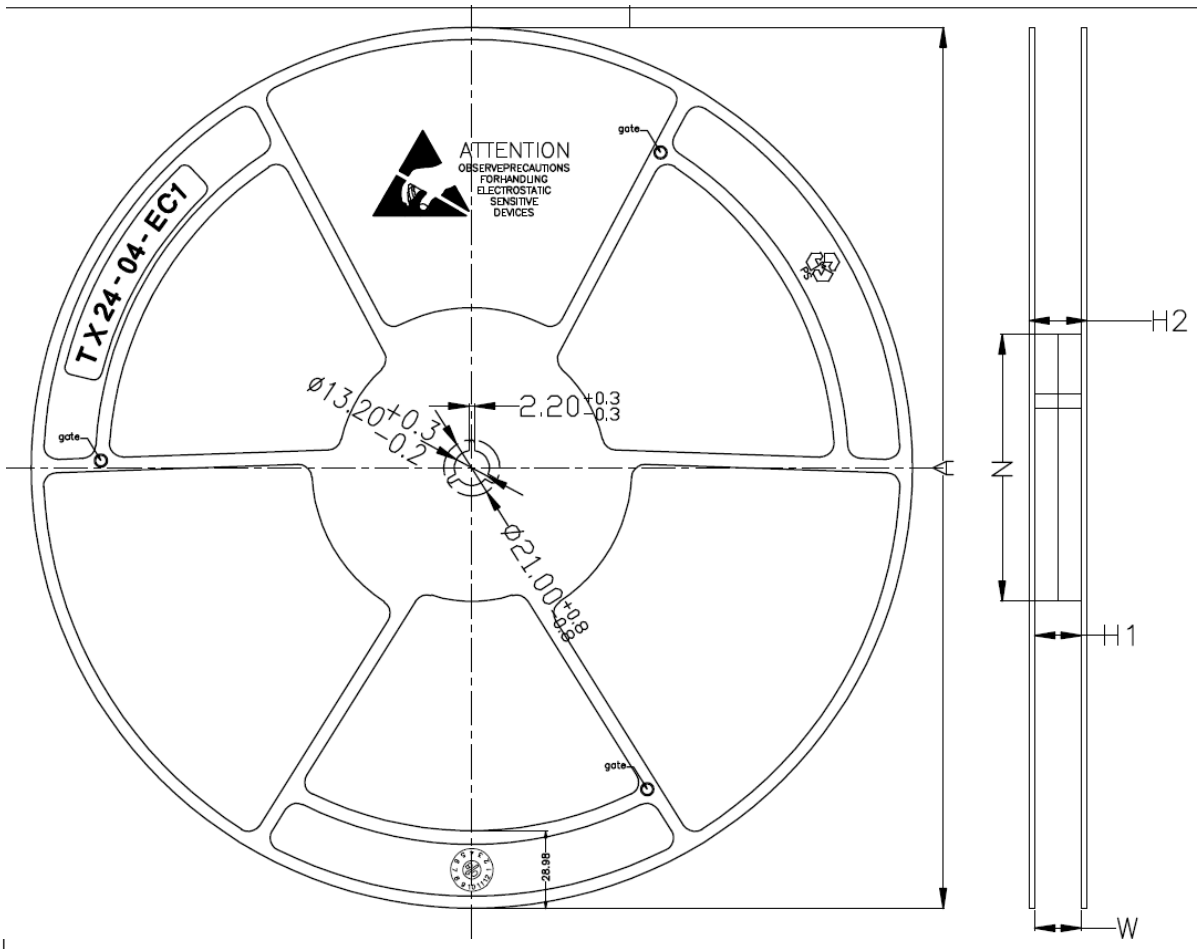
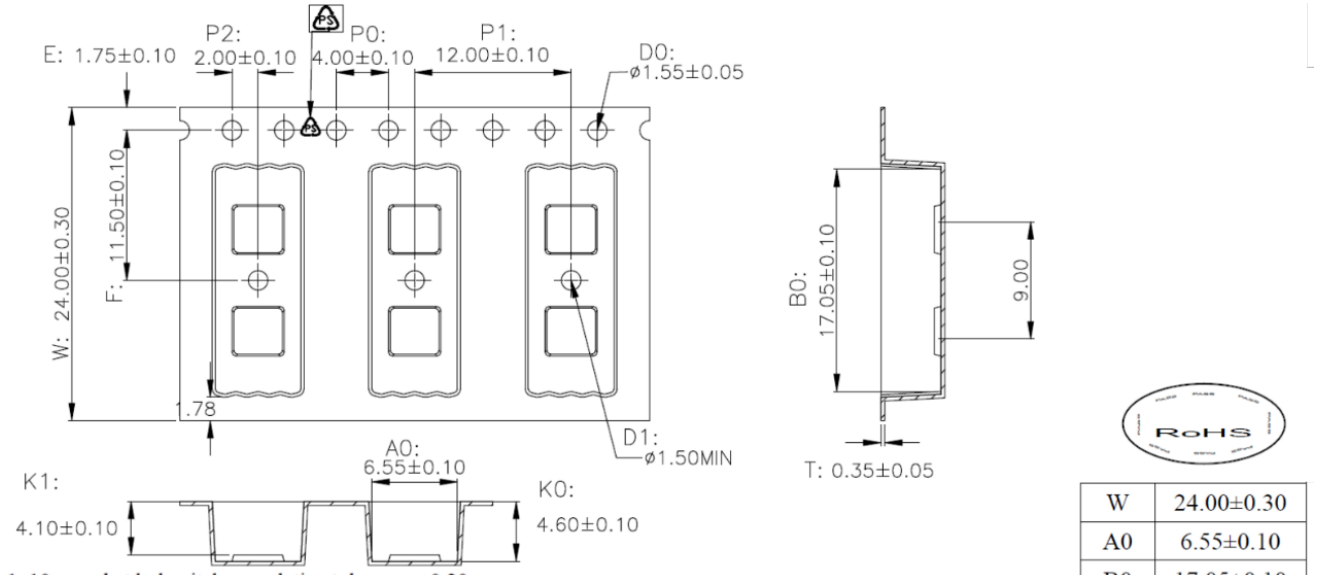


Figure 13. 2 Tape and Reel Information of SOW16



PRODUCT SPECIFICATIONS					
TAPE WIDTH	øA $^{+2}_{-2}$	øN $^{+2}_{-2}$	H1 $^{+2}_{-0}$	H2 $^{+1}_{-1}$	W $^{+3.5}_{-0.2}$
24MM	330	100	24.4	28.6	24.4

NOTES:
1.MATERIAL:DISSIPATIVE(BLACK)
2.FLANGE WARPAGE:3 MM MAXIMUM 5
3.ALL DIMENSIONS ARE IN MM
4.ESD - SURFACE RESISTIVITY-10 TO 10 OHMS/SQ
5.GENERAL TOLERANCE: ±0.25 MM



1. 10 sprocket hole pitch cumulative tolerance ±0.20.
2. Carrier camber is within 1 mm in 250 mm.
3. Material : Black Conductive Polystyrene Alloy.
4. All dimensions meet EIA-481 requirements.
5. Thickness : 0.35±0.05mm.
6. Packing length per 19" reel :130 Meters. (復卷 1: 10)
7. Component load per 13" reel : 1000 pcs.
8. Surface resistivity : 10^5 ~10^{10} Ω/sq.

W	24.00±0.30
A0	6.55±0.10
B0	17.05±0.10
K0	4.60±0.10
K1	4.10±0.10

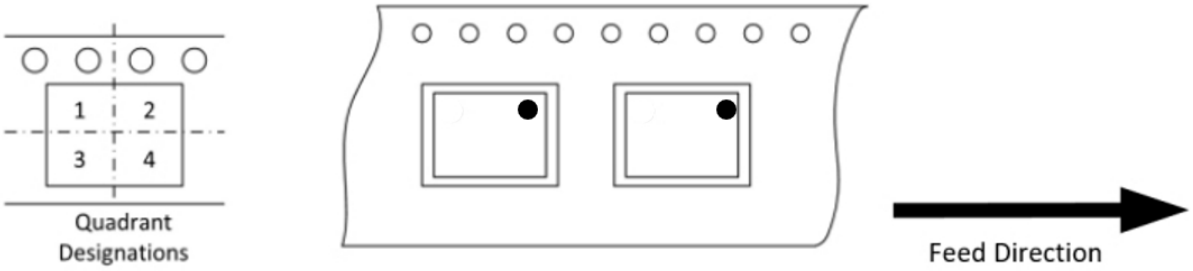


Figure 13. 3 Tape and Reel Information of SOWW8

14. Revision History

Revision	Description	Date
1.0	Original	2023/11/15
1.1	Update SOWW8 Package	2024/5/10

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