NOVOSENSE

NSI6801x

Single-Channel Isolated Gate Driver

Datasheet (EN) 1.0

Product Overview

The NSI6801x is a single-channel isolated gate driver which is pin-compatible for popular opto-coupled gate driver. Where NSI68011 can source 1.5A peak current and sink 2A peak current and NSI68010 can source 0.7A peak current and sink 0.8A peak current. System robustness is supported by 150kV/us minimum common-mode transient immunity (CMTI).

The driver operates with a maximum supply voltage of 32V. While the input circuit imitates the characters of LEDs, it has performance advantages compared to standard opto isolated gate drivers, including better reliability and aging performance, higher working temperature, shorter propagation delay and smaller pulse width distortion.

As a result, the NSI6801x is suitable to replace opto-isolated driver in high reliability, power density and efficiency switching power system.

Key Features

- 5.7kV$_{RMS}$ single channel isolated gate driver
- Pin compatible, drop in upgrade for opto isolated gate drivers
- Rail to rail output or non-rail to rail options
- Driver side supply voltage: up to 32V with UVLO
- 9V or 13V VCC UVLO options
- 1.5A/2A peak source and sink output current(68011)
- 0.7A/0.8A peak source and sink output current(68010)
- High CMTI: ±150kV/us
- 130ns typical propagation delay
- 50ns maximum pulse width distortion
- 35ns part-to-part delay matching
- 15V reverse input voltage supporting interlock
- Operation ambient temperature: -40°C ~125°C
- RoHS & REACH Compliance
- Lead-free component, suitable for lead-free soldering profile: 260°C , MSL3

Safety Regulatory Approvals

- UL recognition: 5700V$_{RMS}$ SOW6 for 1 minute per UL1577
- DIN VDE V 0884-17:2017-01
- CSA component notice 5A
- CQC certification per GB4943.1-2022

Applications

- DC-to-AC solar inverters
- Motor drivers
- UPS and battery chargers
- Isolated DC/DC and AC/DC power supplies

Device Information

Part Number	*Spec Difference*	*Package*	*Body Size*
NSI68010B-DSWAR	9V	SOW6	4.68x7.5x3.18mm
NSI68011C-DSWAR	13V	SOW6	4.68x7.5x3.18mm

Functional Block Diagram

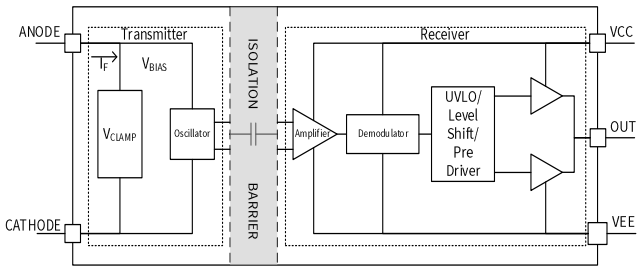


Figure 1. NSI6801x SOW6 Block Diagram

INDEX

1. Pin Configuration and Functions

NSI6801x SOW6 Top View

Table 1.1 NSI6801x Pin Configuration and Description

SYMBOL	PIN NO.		FUNCTION
	NSI68010B	NSI68011C	
ANODE	1	1	Anode of LED emulator
CATHODE	3	3	Cathode of LED emulator
V_{EE}	4	4	Negative output supply rail
V_{OUT}	5	5	Gate-drive output
V_{CC}	6	6	Positive output supply rail
NC	2	2	No Connection

2. Absolute Maximum Ratings

Parameters	Symbol	Min	Max	Unit
Average Input Current	I_{F_AVG}		25	mA
Peak transient Input Current	I_{F_PEAK}		0.2	A
Reverse Input Voltage	V_{R_MAX}		6.5	V
Driver Side Supply Voltage	V_{CC}-V_{EE}	-0.3	35	V
Output Signal Voltage	V_{OUT}	V_{EE}-0.3	V_{CC}+0.3	V
Operating Junction Temperature	T_J	-40	150	°C
Storage Temperature	T_{stg}	-65	150	°C

3. ESD Ratings

	Ratings	Value	Unit
Electrostatic discharge	Human body model (HBM), per AEC-Q100-002-RevD ● All pins	±2000	V
	Charged device model (CDM), per AEC-Q100-011-RevB ● All pins	±1000	V

4. Recommended Operating Conditions

Parameters	Symbol	Min	Max	Unit
Input Current (ON)	$I_{F(ON)}$	7	16	mA
Input Voltage (OFF)	$V_{F(off)}$	-5.5	0.9	V
Driver Side Supply Voltage (NSI6801xC)	V_{CC}-V_{EE}	14	32	V
Driver Side Supply Voltage (NSI6801xB)	V_{CC}-V_{EE}	10	32	V
Ambient Temperature	T_A	-40	125	°C

5. Thermal Information

Parameters	Symbol	NSI6801x	Unit
Junction–to-ambient thermal resistance	$R_{\theta JA}$	125	°C/W
Junction–to-top characterization parameter	Ψ_{JT}	30	°C/W

6. Specifications

6.1. DC Electrical Characteristics

Unless otherwise noted, Typical values are at V_{CC} =15V, V_{EE}=GND, T_A=25°C. All min and max specifications are at T_A=-40°C to 125°C, V_{CC}=14V to 32V, V_{EE}=GND, $I_{F(ON)}$=7 mA to 16 mA, $V_{F(off)}$= –5.5V to 0.8V

Parameter	Symbol	Min	Typ	Max	Unit	Condition
Driver Side Supply						
High Level Supply Current	I_{CCH}		1.7	2.5	mA	I_F=10mA, I_{OUT}=0mA
Low Level Supply Current	I_{CCL}		1.6	2.5	mA	V_F=0V, I_{OUT}=0mA
Driver Side Supply UVLO Threshold (NSI68010B, 9V UVLO Level)						
VCC UVLO Rising Threshold	V_{CC_ON}	7.8	8.5	9.2	V	I_F=10mA
VCC UVLO Falling Threshold	V_{CC_OFF}	7.1	7.7	8.5	V	
VCC UVLO Hysteresis	V_{CC_HYS}		0.8		V	
Driver Side Supply UVLO Threshold (NSI68011C, 13V UVLO Level)						
VCC2 UVLO Rising Threshold	V_{CC2_ON}	11	12.6	13.5	V	I_F=10mA
VCC2 UVLO Falling Threshold	V_{CC2_OFF}	10	11.6	12.5	V	
VCC2 UVLO Hysteresis	V_{CC2_HYS}		1		V	
Input Pin Characteristic						
Input Forward Threshold Current Low to High	I_{FLH}	1.5	2.7	5.5	mA	V_{OUT}>5V, Cg=1nF
Threshold Input Voltage High to Low	V_{FHL}	0.9			V	V_{OUT}<5V, Cg=1nF
Input Forward Voltage	V_F	1.5	2.1	2.5	V	I_F=10mA
Temp Coefficient of Input Forward Voltage	$\Delta V_F/\Delta T$		0.34		mV/°C	I_F=10mA
Input Reverse Breakdown Voltage	V_R	6.5			V	I_R=10μA
Input Capacitance	C_{IN}		17		pF	f=1MHz
Output Pin Characteristic(NSI68010B, 9V UVLO Level)						
High Level Output Voltage	V_{OH}	V_{CC}-2	V_{CC}-1.8		V	I_{OUT}=-50mA, I_F=10mA
Low Level Output Voltage	V_{OL}		170	350	mV	I_{OUT}=50mA, V_F=0V
High Level Peak Output Current	I_{OH}		0.7		A	V_{CC}=15V, pulse width<10μs
Low Level Peak Output Current	I_{OL}		0.8		A	V_{CC}=15V, pulse width<10μs
Output Pin Characteristic(NSI68011C, 13V UVLO Level)						
High Level Output Voltage	V_{OH}		V_{CC}-0.2		V	I_{OUT}=-50mA, I_F=10mA
Low Level Output Voltage	V_{OL}		70		mV	I_{OUT}=50mA, V_F=0V
High Level Peak Output Current	I_{OH}		1.5		A	V_{CC}=15V, pulse width<10μs
Low Level Peak Output Current	I_{OL}		2		A	V_{CC}=15V, pulse width<10μs

6.2. Switching Electrical Characteristics

(Unless otherwise noted, Typical values are at V_{CC} =15V, V_{EE}=GND, T_A=25°C. All min and max specifications are at T_A=-40°C to 125°C, V_{CC}=14V to 32V, V_{EE}=GND, $I_{F(ON)}$=7 mA to 16 mA, $V_{F(off)}$= –5.5V to 0.8V)

Parameter	Symbol	Min	Typ	Max	Unit	Condition
Propagation Delay	t_{pLH}		140	160	ns	C_{LOAD}=1nF, f=20kHz (50% Duty Cycle)
Propagation Delay	t_{pHL}		130	150	ns	
Pulse Width Distortion $\|t_{PLH}-t_{PHL}\|$	t_{PWD}			50	ns	
Propagation Delay Difference Between Any Two Parts ($t_{pHL}-t_{pLH}$) (1)	PDD	-35		35	ns	
Output Rise Time (20% to 80%)	t_R		43		ns	
Output Fall Time (80% to 20%)	t_F		50		ns	
Common Mode transient Immunity	CMTI	150			kV/μs	Verified by design

(1) The difference between t_{PHL} and t_{PLH} between any two parts under the same test condition, ensured by characterization.

6.3. Typical Performance characteristics

Vcc=15V, T_A=25°C. Output has no load unless otherwise noted.

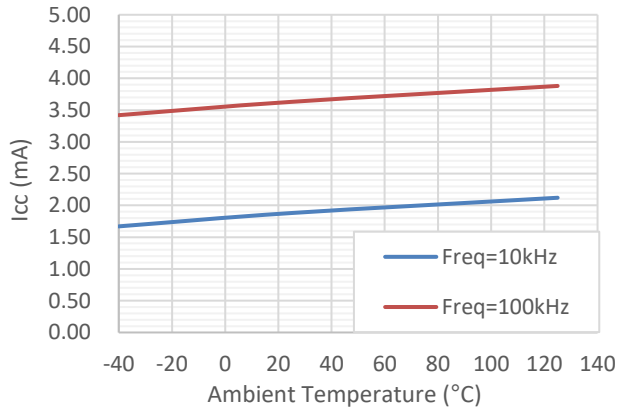


Figure 6.1 Supply currents versus Temperature

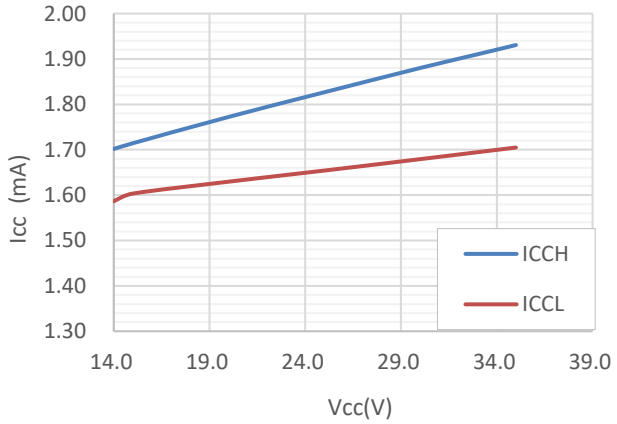


Figure 6.2 Supply current versus Supply Voltage

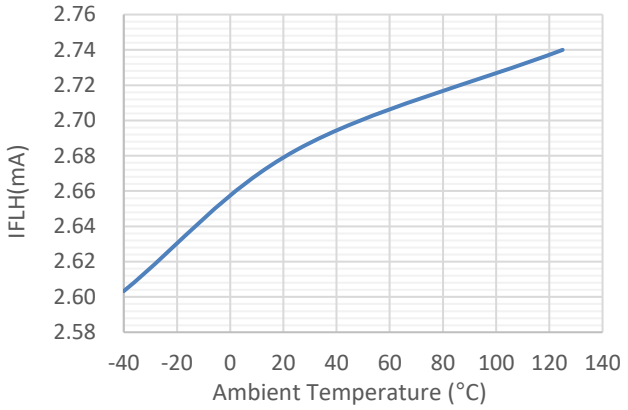


Figure 6.3 Forward threshold current versus Temperature

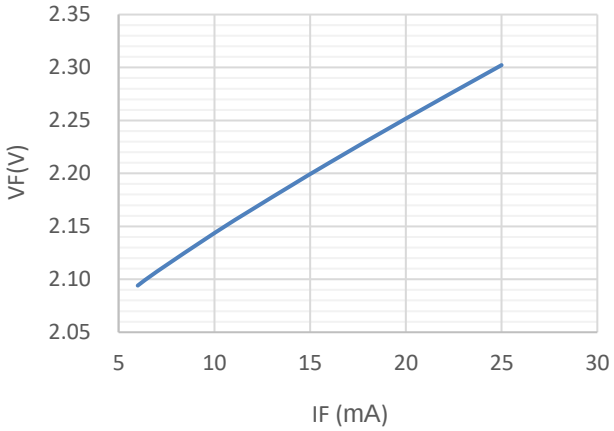


Figure 6.4 Forward current versus Forward voltage drop

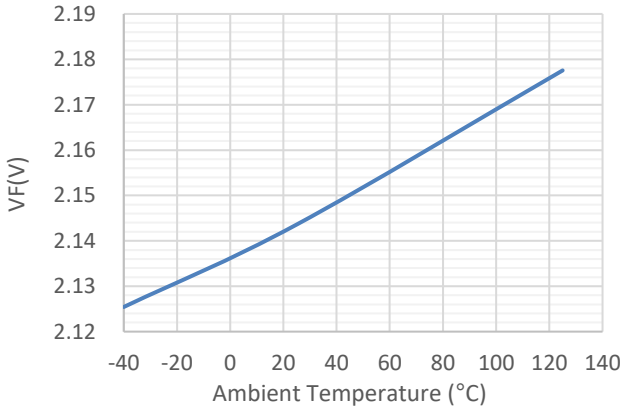


Figure 6.5 Forward voltage drop versus Temperature

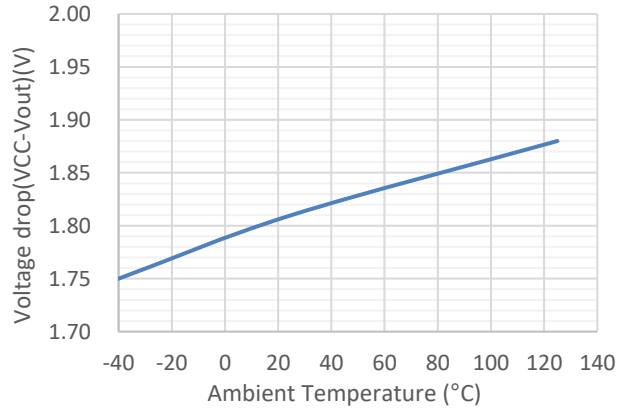


Figure 6.6 V_{OH} versus Temperature of 68010

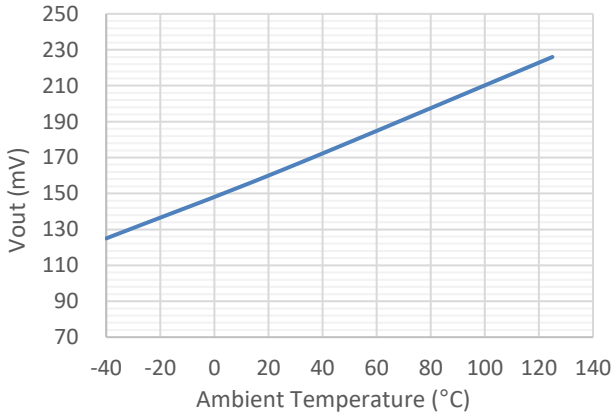


Figure 6.7 V_{OL} versus Temperature of 68010

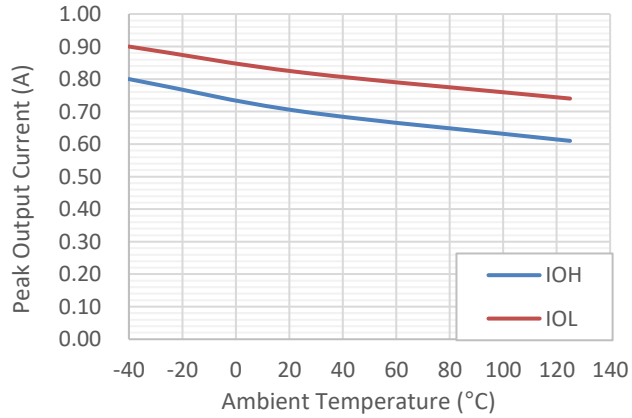


Figure 6.8 Output drive currents versus Temperature of 68010

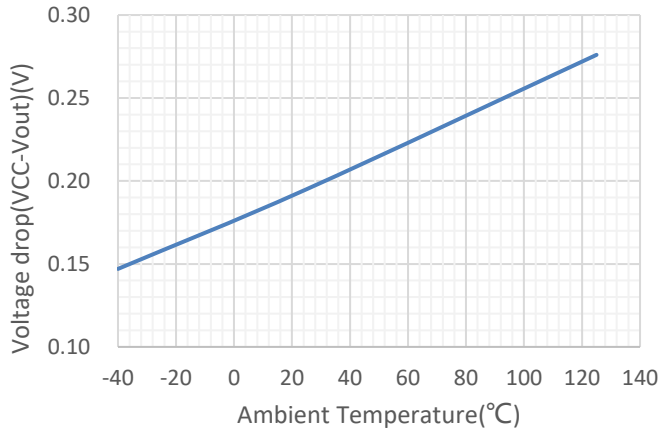


Figure 6.9 V_{OH} versus Temperature of 68011

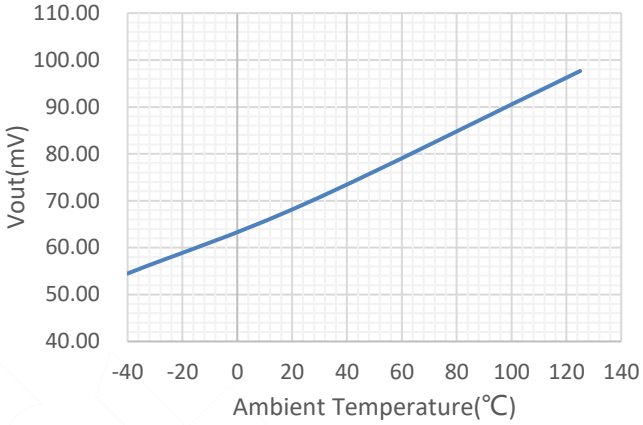


Figure 6.10 V_{OL} versus Temperature of 68011

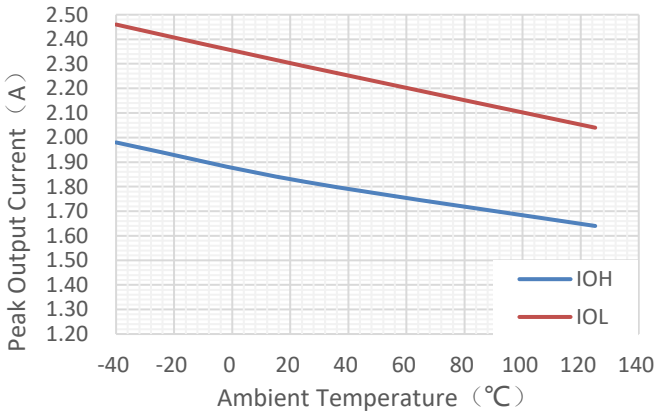


Figure 6.11 Output drive currents versus Temperature of 68011

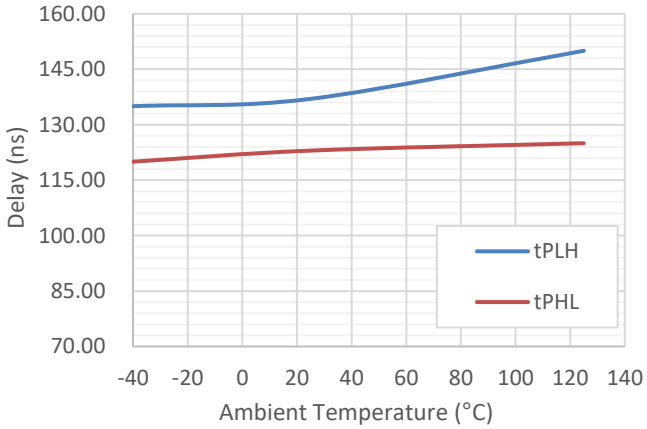


Figure 6.12 Propagation delay versus Temperature

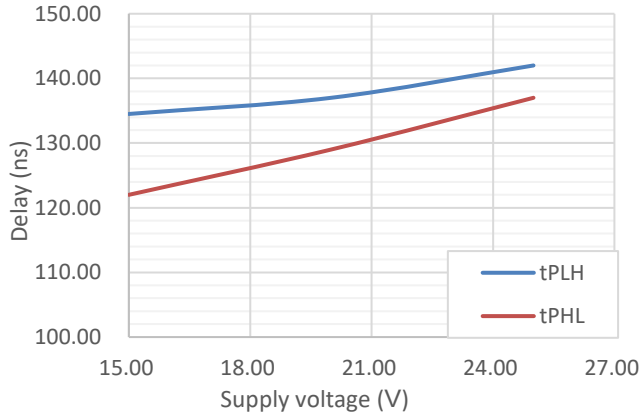


Figure 6.13 Propagation delay versus Supply voltage

6.4. Parameter Measurement Information

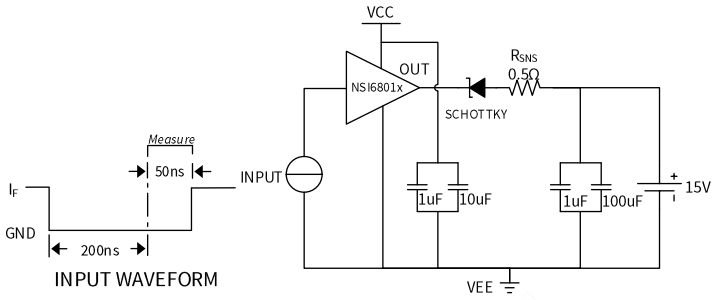


Figure 6.14 I_{OL} Sink Current Test Circuit

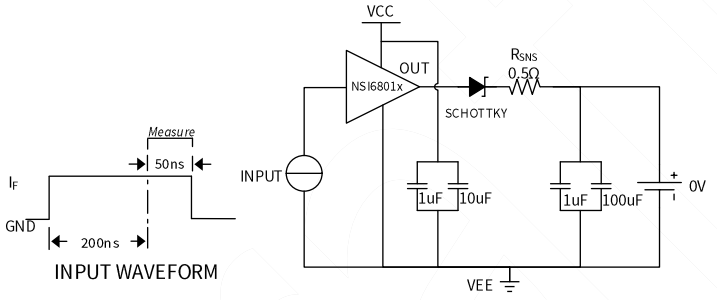


Figure 6.15 I_{OH} Source Current Test Circuit

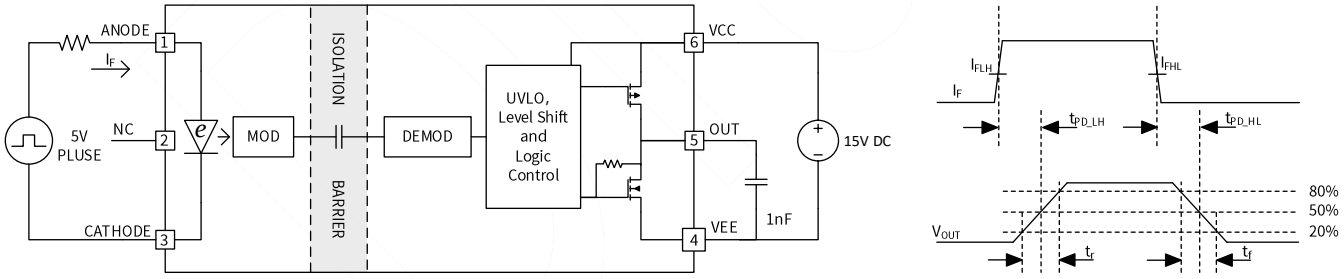


Figure 6.16 I_F to V_{OUT} Propagation Delay, Rise Time and Fall Time

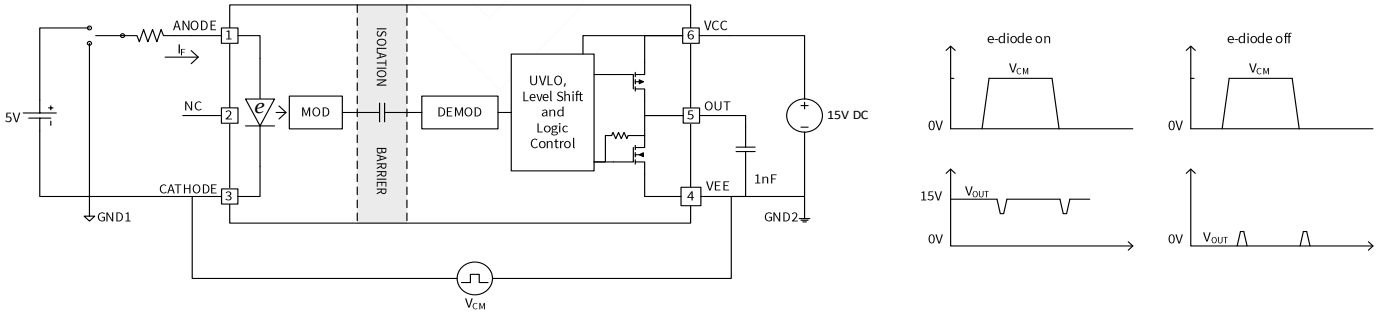


Figure 6.17 Common Mode transient Immunity Test Circuit

7. High Voltage Feature Description

7.1. Insulation and Safety Related Specifications

Parameters	*Symbol*	*Value*	*Unit*	*Comments*
Minimum External Air Gap (Clearance)	CLR	8	mm	Shortest terminal-to-terminal distance through air
Minimum External Tracking (Creepage)	CPG	8	mm	Shortest terminal-to-terminal distance across the package surface
Distance Through Insulation	DTI	20	μm	Minimum internal gap
Tracking Resistance (Comparative Tracking Index)	CTI	600	V	DIN EN 60112 (VDE 0303-11); IEC 60112
Material Group		I		IEC 60664-1

7.2. Insulation Characteristics for SOW6 Package

Description	Test Condition	Symbol	Value	Unit
Overvoltage Category per IEC60664-1	For Rated Mains Voltage ≤ 600V_{RMS}		I to IV	
	For Rated Mains Voltage ≤ 1000V_{RMS}		I to III	
Climatic Category			40/125/21	
Pollution Degree per DIN VDE 0110, Table 1			2	
DIN EN IEC 60747-17 (VDE 0884-17)				
Maximum Working Isolation Voltage		V_{IOWM}	1500	V_{RMS}
			2121	V_{DC}
Maximum Repetitive Isolation Voltage		V_{IORM}	2121	V_{PEAK}
Apparent Charge	Method a, after Input/output safety test subgroup 2/3, Vini=V_{IOTM}, t_{ini} = 60 s ,$V_{pd(m)}$=1.2*V_{IORM}, t_m=10s.	q_{pd}	<5	pC
	Method a, after environmental tests subgroup 1, Vini=V_{IOTM}, t_{ini}=60s ,$V_{pd(m)}$=1.6*V_{IORM}, t_m=10s	q_{pd}	<5	pC
	Metod b, routine test (100% production) and preconditioning (type test);V_{ini}=1.2*V_{IOTM}, t_{ini}=1s $V_{pd\ (m)}$=1.875*V_{IORM}, t_m=1s	q_{pd}	<5	pC
Maximum transient Isolation Voltage	t = 60 s	V_{IOTM}	8000	V_{PEAK}
Maximum impulse voltage	Tested in air, 1.2/50μs waveform per IEC62368-1	V_{imp}	6250	V_{PEAK}
Maximum Surge Isolation Voltage	Test method per IEC62368-1, 1.2/50μs waveform, V_{IOSM}≥V_{IMP} × 1.3	V_{IOSM}	10000	V_{PEAK}
Isolation Resistance	VIO=500V, T_{amb}=25℃	R_{IO}	>10^{12}	Ω
	V_{IO} =500V at T_A=T_S=150°C		>10^{9}	Ω
	V_{IO} =500V at 100°C≤T_A≤125°C		>10^{11}	Ω
Isolation Capacitance	f = 1MHz	C_{IO}	1	pF
UL1577				
Insulation voltage per UL	V_{TEST} = V_{ISO}, t = 60 s (qualification), V_{TEST} = 1.2 × V_{ISO}, t = 1 s (100% production test)	V_{ISO}	5700	V_{RMS}

7.3. Safety-Limiting Values for SOW6 Package

Description	*Test Condition*	*Symbol*	*Value*	*Unit*
Maximum Safety Temperature		T_S	150	°C
Safety Input, Output, or Total Power	$R_{\theta JA}$=125°C/W, T_J=150°C, T_A=25°C	P_S	750	mW
Safety Input, Output, or Supply Current	$R_{\theta JA}$=125°C/W, V_{CC}=15V, T_J=150°C, T_A=25°C	I_S	50	mA
	$R_{\theta JA}$=125°C/W, V_{CC}=30V, T_J=150°C, T_A=25°C	I_S	25	mA

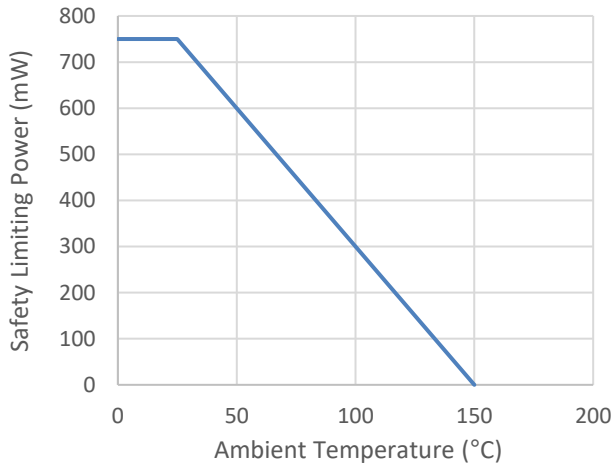


Figure 7.1 Thermal Derating Curve for Limiting Power per DIN VDE V 0884-17 for SOW6 Package

7.4. Regulatory Information for SOW6 Package

UL		*VDE*	*CQC*
UL 1577 Component Recognition Program	Approved under CSA Component Acceptance Notice 5A	Certified according to DIN EN IEC 60747-17 (VDE 0884-17)	Certified according to GB4943.1-2022
Single Protection, 5700V_{RMS} Isolation Voltage	Single Protection, 5700V_{RMS} Isolation voltage	Reinforced Insulation V_{IORM}=2121V_{PEAK}, V_{IOTM}=8000V_{PEAK}, V_{IOSM}=10000V_{PEAK}	Reinforced Insulation
Certificate No.E500602		Certificate No.40052820	Certificate No.CQC21001289930

8. Function Description

The NSI6801x is a single-channel isolated gate driver which is pin-compatible for popular opto-coupled gate driver. The integrated galvanic isolation between control input logic and driving output stage grants additional safety. The device can source 1.5A and sink 2A peak current, which can drive IGBTs, power MOSFETs and SiC MOSFETs in many applications such as motor control systems, solar inverters and power supplies.

Functional Block Diagram

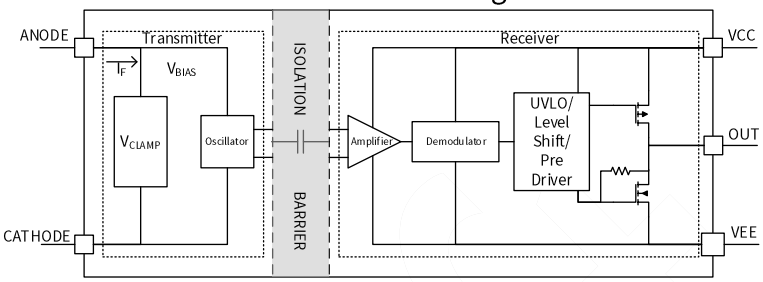


Figure 8.1 NSI6801x Functional Block Diagram

8.1. Truth Tables

Table 8.1 Driver Function Table (1)

e-diode	*V_{CC} status*	*Outputs*
X	Powered Down	L
$I_F > I_{FLH}$	Powered Up	H
$V_F < V_{FHL}$	Powered Up	L

(1) H= Logic High; L= Logic Low; X= Irrelevant

8.2. Output Stage

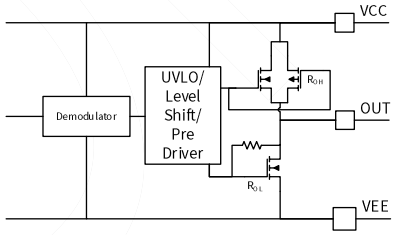


Figure 8.2 NSI68011 Output Stage

Table 8.2 NSI68011 Output Stage On-Resistance

Part number	*R_{NMOS}*	*R_{OH}*	*R_{OL}*	*Unit*
NSI68011C	2.7	4	1.4	Ω

The NSI68011 has P-channel and N-channel MOSFET in parallel to pull up the OUT pin when turning on external power transistor. During DC measurement, only the P-channel MOSFET is conducting. The measurement result R_{OH} represents the on-resistance of P-channel MOSFET.

The voltage and current of external power transistor drain to source or collector to emitter change during turn on. At that time, the NSI68011 N-channel MOSFET turns on to pull up OUT more quickly. It results external power transistor faster turn on time, lower turn on power loss, also leads to smaller temperature increase of NSI68011. The equivalent pull-up resistance of NSI68011 is the parallel combination $R_{OH} \parallel R_{NMOS}$. The result is quite small, indicating the strong driving capability of NSI68011.

The pull-down structure of NSI6801x is simply composed of an N-channel MOSFET with on-resistance of R_{OL}. The result is quite small, indicating the strong driving capability of NSI68011.

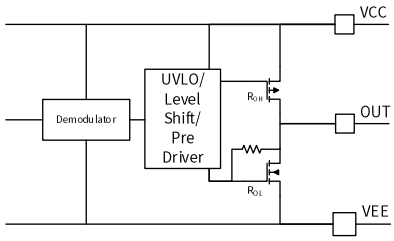


Figure 8.3 NSI68010 Output Stage

Table 8.3 NSI68010 Output Stage On-Resistance

Part number	*R_{OH}*	*R_{OL}*	*Unit*
NSI68010B	36	3.4	Ω

The NSI68010 use N-channel MOSFET to pull up the OUT pin when turning on external power transistor. The measurement result R_{OH} represents the on-resistance of N-channel MOSFET.

The voltage and current of external power transistor drain to source or collector to emitter change during turn on. At that time, the NSI68010 N-channel MOSFET turns on to pull up OUT more quickly. It results external power transistor faster turn on time, lower turn on power loss, also leads to smaller temperature increase of NSI68010. The result of the pull-up resistance R_{OH} is quite small, indicating the strong driving capability of NSI68010.

The pull-down structure of NSI68010 is simply composed of an N-channel MOSFET with on-resistance of R_{OL}. The result is quite small, indicating the strong driving capability of NSI68010.

8.3. V_{CC} and Under Voltage Lock Out (UVLO)

The lower limit of driver side supply voltage (V_{CC}) is determined by the internal UVLO protection feature of the device. V_{CC} voltage should not fall below the UVLO threshold for normal operation, or else the gate-driver outputs can become clamped low.

A local bypass capacitor should be placed between the V_{CC} and V_{EE} pins, with a value of 220nF to 10μF for device biasing. An additional 100nF capacitor in parallel with the device biasing capacitor is recommended for high frequency filtering. Both capacitors should be positioned as close to the device as possible. Low-ESR, ceramic surface-mount capacitors are recommended.

8.4. Active Pull-Down

The Active Pull-Down feature ensures a safe IGBT or MOSFET off-state if V_{CC} is not connected to the power supply. When V_{CC} is floating, the driver output is held low and clamping V_{OUT} pin to approximately 1.9V higher than V_{EE}.

8.5. Short Circuit Clamping

During short circuit the gate voltage of IGBT or MOSFET tends to rise because of the feedback via the Miller capacitance. The diode between V_{OUT} and V_{CC} pins inside the driver limits this voltage to a value slightly higher than the supply voltage. A maximum current of 500 mA may be fed back to the supply through this path for 10 μs. If higher currents are expected or tighter clamping is desired external Schottky diodes may be added.

9. Application Note

9.1. Typical Application

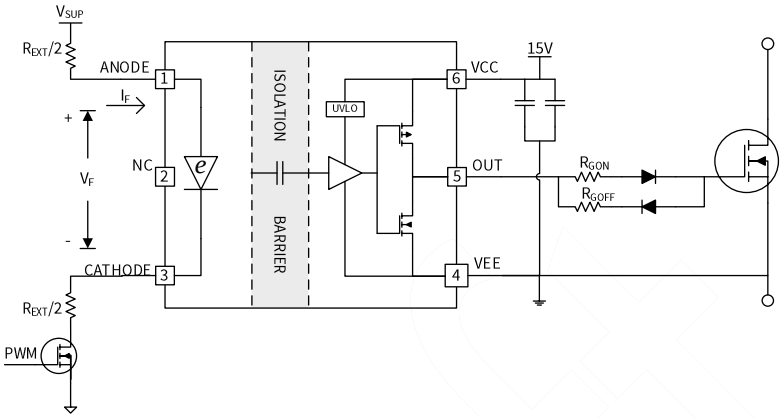


Figure 9.1 NSI6801x typical application circuit with NMOS driving input stage

Bypassing capacitors connecting between V_{CC} and V_{EE} are needed to achieve reliable performance. To filter noise, 0.1μF/50V ceramic capacitor is recommended to place as close as possible to NSI6801x. To support high peak currents when turning on external power transistor, additional 10μF/50V ceramic capacitor is recommended. If the V_{CC} power supply is located long distance from the IC, bigger capacitance is needed.

NSI6801x requires 7mA to 16mA bias current that flows into the e-diode for normal operation. The PWM from MCU is not suitable to provide such current directly and external circuit is needed. In Figure 9.1, one NMOS is used with split input resistors. Another input drive method is using one buffer, as shown in Figure 9.2. The details to calculate input drive parameters are in Chapter 9.3.

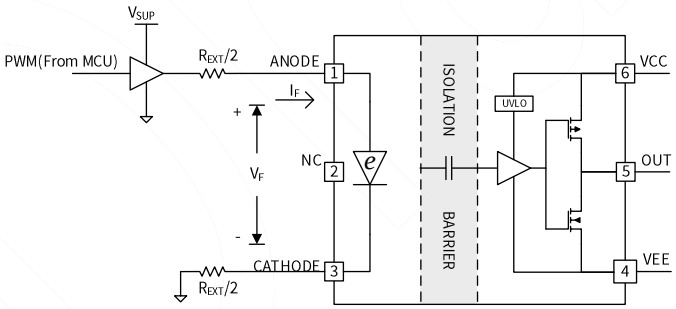


Figure 9.2 NSI6801x typical application circuit with one buffer driving input stage

9.2. Interlock Protection

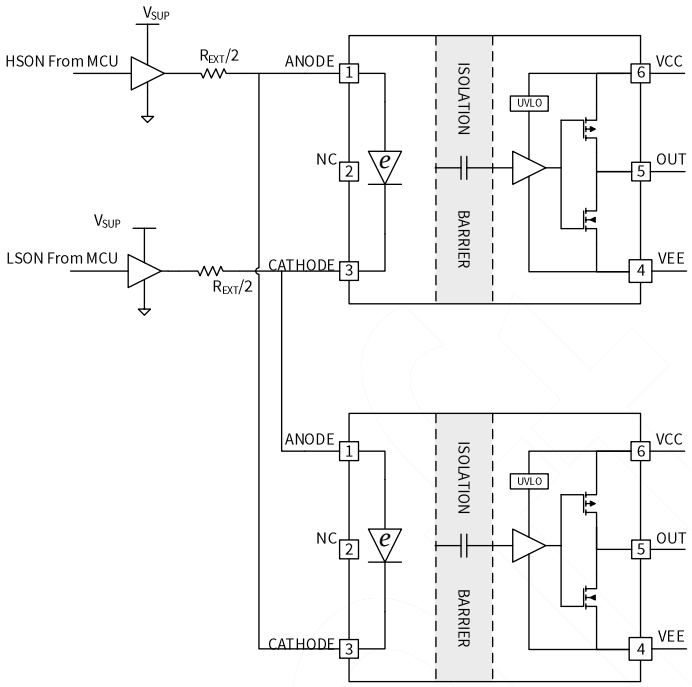


Figure 9.3 Interlock Protection using NSI6801x

For applications to drive power transistors in half bridge configuration, two NSI6801x can be used. Interlock protection is possible as shown in Figure 9.3. If the controller has some mistake, leading to negative dead time, the output PWM of NSI6801x is adjusted to avoid power transistor shoot through. The input side reverse breakdown voltage of NSI6801x is greater than 15V, which supports interlock protection of 3.3V or 5V PWM signal source.

9.3. Selecting Input Resistor

The recommended forward current range for NSI6801 is 7mA to 16mA. The value of input resistor, buffer supply voltage and buffer internal resistance influence the forward current, as shown in Equation (1). In Figure 9.1, R_{IN1} is the on-resistance of the external NMOS. In Figure 9.2, R_{IN2} is the buffer output impedance in output "High" state. In Figure 9.3, R_{IN3} is the summary of buffer output impedance in "High" and "Low" state.

$$R_{EXT} = \frac{V_{SUP}-V_F}{I_F} - R_{INx} \quad (1)$$

The parameter variation needs to be taken into consideration when selecting input resistor. Table 9.1 lists parameter variation in this example. Manufacturer's tolerance for R_{EXT} is 2%.

Table 9.1 External parameters range when calculating input resistor

Parameters	*Min*	*Typ*	*Max*
NSI6801 forward current I_F	7mA	10mA	16mA
NSI6801 forward voltage V_F	1.8V	2.1V	2.4V
Buffer supply voltage V_{SUP}	5V*95%	5V	5V*105%
R_{IN1}	0.25Ω	/	1Ω
R_{IN2}	13Ω	18Ω	22Ω
R_{IN3}	9Ω	14Ω	18Ω

R_{EXT} caculated based on these parameters above is as follows:

$$R_{EXT\_min} = \left(\frac{V_{SUP\_max} - V_{F\_min}}{I_{F\_max}} - R_{INx\_min}\right)/(1 - 2\%) \quad (2)$$

$$R_{EXT\_typ} = \frac{V_{SUP\_typ} - V_{F\_typ}}{I_{F\_typ}} - R_{INx\_typ} \quad (3)$$

$$R_{EXT\_max} = \left(\frac{V_{SUP\_min} - V_{F\_max}}{I_{F\_min}} - R_{INx\_max}\right)/(1 + 2\%) \quad (4)$$

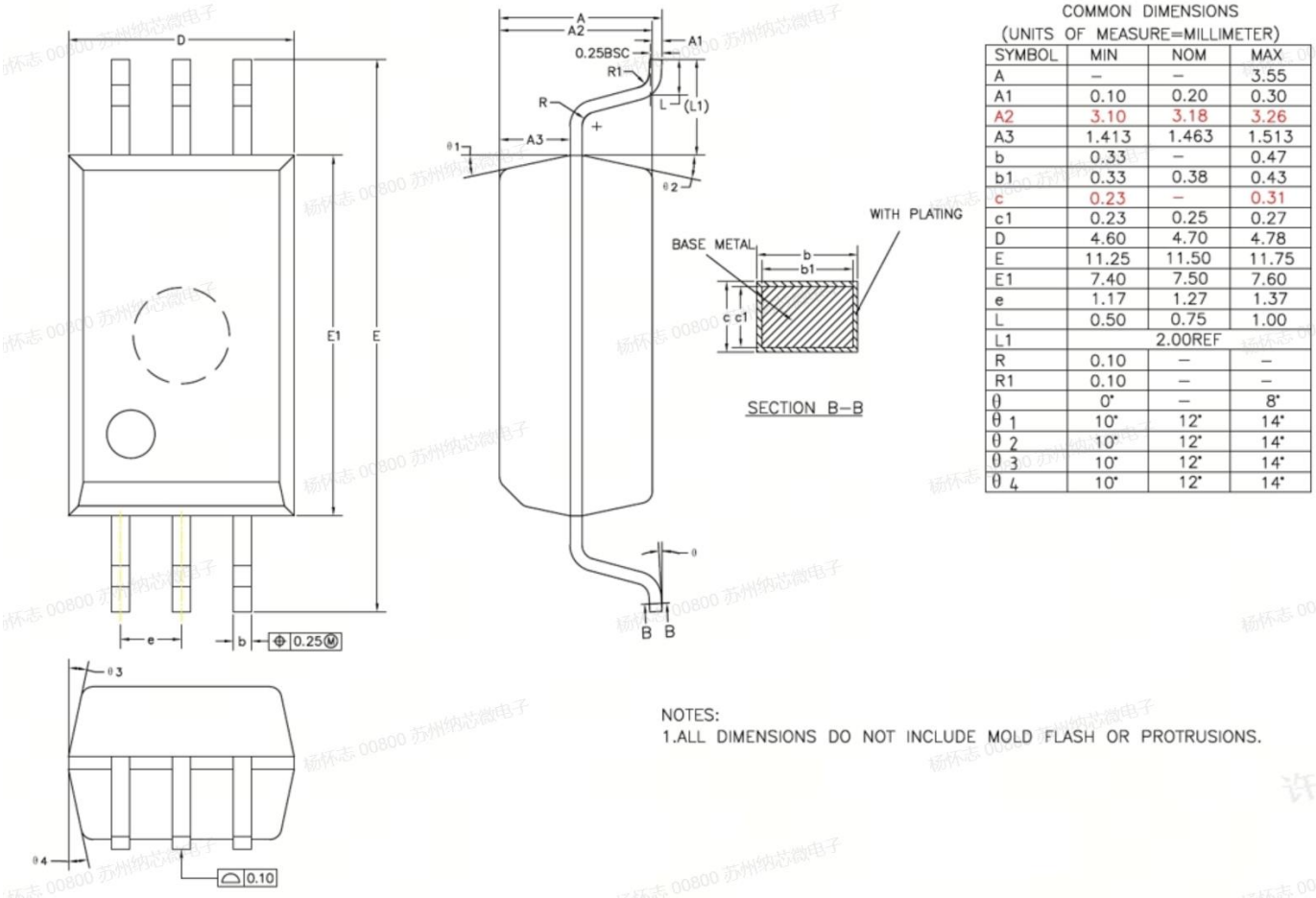
Where R_{INx}=R_{IN1} or R_{IN2} or R_{IN3} is determined by topology.

9.4. PCB Layout

Careful PCB layout is essential for optimal performance. Some key guidelines are:

- The bypass capacitors should be placed close to NSI6801x, between V_{CC} to V_{EE}.
- There is high switching current that charges and discharges the gate of external power transistor, leading to EMI and ring issues. The parasitic inductance of this loop should be minimized, by decreasing loop area and place NSI6801x close to power transistor.
- Place large amount of copper connecting to V_{EE} pin and V_{CC} pin for thermal dissipation, with priority on V_{EE} pin. If the system has multi V_{EE} or V_{CC} layers, use multiple vias of adequate size for connection.
- To ensure isolation performance between primary and secondary side, the space under the chip should keep free from planes, traces, pads or via.

10. Package Information



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	–	–	3.55
A1	0.10	0.20	0.30
A2	3.10	3.18	3.26
A3	1.413	1.463	1.513
b	0.33	–	0.47
b1	0.33	0.38	0.43
c	0.23	–	0.31
c1	0.23	0.25	0.27
D	4.60	4.70	4.78
E	11.25	11.50	11.75
E1	7.40	7.50	7.60
e	1.17	1.27	1.37
L	0.50	0.75	1.00
L1		2.00REF	
R	0.10	–	–
R1	0.10	–	–
θ	0°	–	8°
θ 1	10°	12°	14°
θ 2	10°	12°	14°
θ 3	10°	12°	14°
θ 4	10°	12°	14°

Figure 10.1 SOW6 Package Shape and Dimension in millimeters

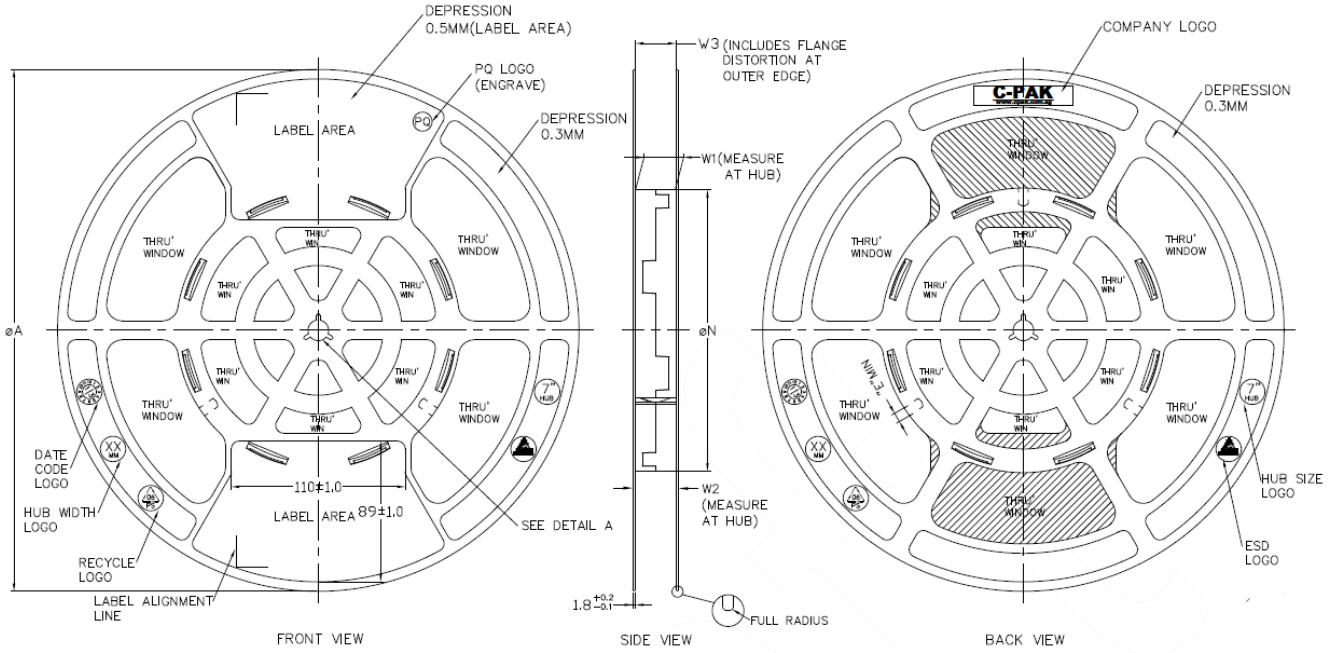
11. Ordering Information

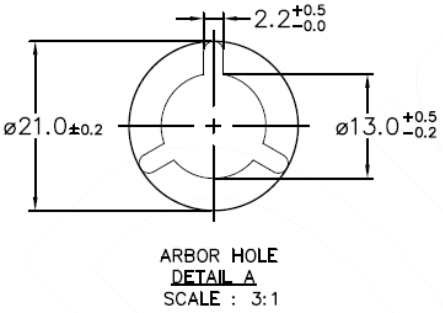
Part No.	*Driver-side UVLO TYP.*	*Temperature*	*MSL*	*Package*	*Body Size(mm)*	*Auto-motive*
NSI68010B-DSWAR	9V	-40 to 125°C	3	SOW6	4.68x7.5x3.18	NO
NSI68011C-DSWAR	13V	-40 to 125°C	3	SOW6	4.68x7.5x3.18	NO

12. Documentation Support

Part Number	*Product Folder*	*Datasheet*	*Technical Documents*	*Isolated Driver Selection Guide*
NSI6801x	Click here	Click here	Click here	Click here

13. Tape and Reel Information

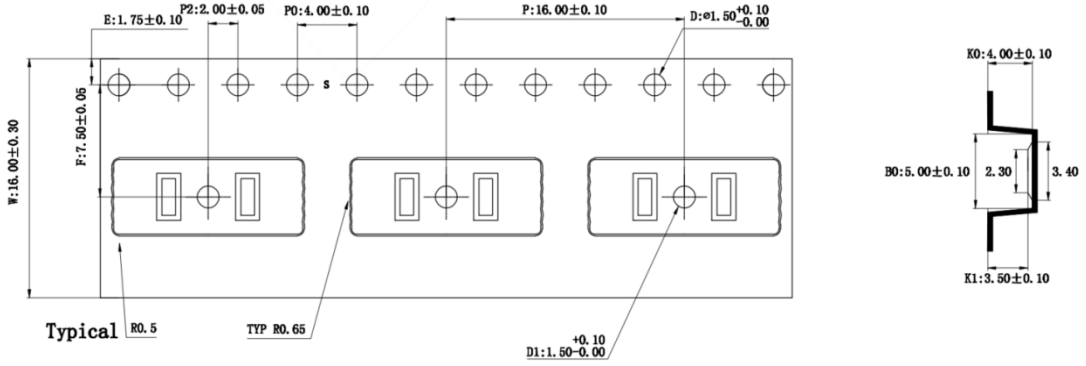




PRODUCT SPECIFICATION						
TAPE WIDTH	øA ±2.0	øN ±2.0	W1	W2 (MAX)	W3	E (MIN)
08MM	330	178	8.4 +1.5 -0.0	14.4	SHALL ACCOMMODATE TAPE WIDTH WITHOUT INTERFERENCE	5.5
12MM	330	178	12.4 +2.0 -0.0	18.4		5.5
16MM	330	178	16.4 +2.0 -0.0	22.4		5.5
24MM	330	178	24.4 +2.0 -0.0	30.4		5.5
32MM	330	178	32.4 +2.0 -0.0	38.4		5.5

SURFACE RESISTIVITY			
LEGEND	SR RANGE	TYPE	COLOUR
A	BELOW 10^{12}	ANTISTATIC	ALL TYPES
B	10^{6} TO 10^{11}	STATIC DISSIPATIVE	BLACK ONLY
C	10^{5} & BELOW 10^{5}	CONDUCTIVE (GENERIC)	BLACK ONLY
E	10^{9} TO 10^{11}	ANTISTATIC (COATED)	ALL TYPES

Figure 13.1 Reel Information



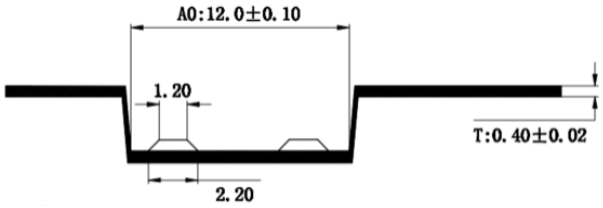


Figure 13.2 Tape Information of SOW6

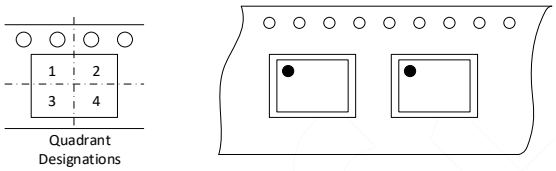


Figure 13.3 Quadrant Designation for Pin1 Orientation in Tape

14. Revision History

Revision	Description	Date
1.0	Initial version	2023/10/13

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