Product Overview

NCA3485 is a half-duplex RS-485 transceiver. NCA3491 is a full-duplex RS-485 transceiver.

The devices have a 1/8-unit-load receiver input impedance that allows up to 256 transceivers on the bus. The data rate of the device is up to 12Mbps. The device is slew limited to reduce EMI and reflections with improperly terminated transmission line.

The Bus pins are protected from ±10kV system level ESD to GND. These devices feature fail-safe circuitry, which guarantees a logic-high receiver output when the receiver inputs are open or shorted.

Key Features

- Power supply voltage: 3.0V to 5.5V

- High system level EMC performance:

    Bus Pins meet IEC61000-4-2 ±10kV ESD

- Fail-safe protection receiver

- Up to 256 transceivers on the bus

- Operation temperature: -40℃~125℃

- RoHS-compliant packages:

    SOP8

    SOP14

Applications

- Industrial automation system

- RS-485 communication

Device Information

Part Number	Package	Body Size
NCA3485-DSPR	SOP8	4.90mm × 3.90mm
NCA3491-DSPKR	SOP14	8.63mm × 3.90mm

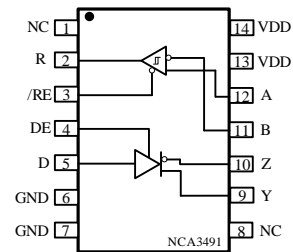## Functional Block Diagrams
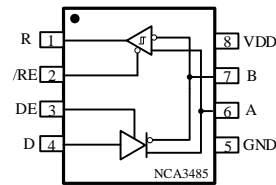
Figure 1. NCA3485 Block Diagrams

Figure 2. NCA3491 Block Diagrams

INDEX

1. Pin Configuration and Functions
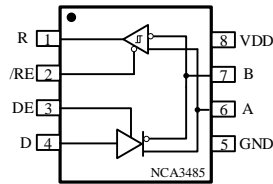
Figure 1.1 NCA3485 Package

Table1.1 NCA3485 Pin Configuration and Description

NSi83085E PIN NO.	SYMBOL	FUNCTION
1	R	Receive output
2	/RE	Receive enable input. This is an active low input.
3	DE	Driver enable input. This is an active high input
4	D	Driver transmit data input.
5	GND	Ground.
6	A	Noninverting Driver Output/Receiver Input. When the driver is disabled, or when VDD is powered down, Pin A is put into a high impedance state to avoid overloading the bus.
7	B	Inverting Driver Output/Receiver Input. When the driver is disabled, or when VDD is powered down, Pin B is put into a high impedance state to avoid overloading the bus.
8	VDD	Power Supply.

Figure 1.2 NCA3491 Package

Table1.2 NCA3491 Pin Configuration and Description

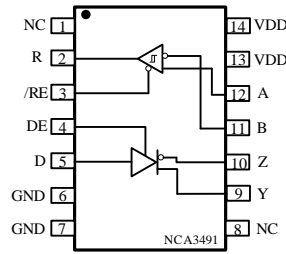| NSi83085E PIN NO.	SYMBOL	FUNCTION
1	NC	No Connection.
2	R	Receive output
3	/RE	Receive enable input. This is an active low input.
4	DE	Driver enable input. This is an active high input
5	D	Driver transmit data input.
6	GND	Ground.
7	GND	Ground.
8	NC	No Connection.
9	Y	Noninverting Driver Output. When the driver is disabled, or when VDD is powered down, Pin Y is put into a high impedance state to avoid overloading the bus.
10	Z	Inverting Driver Output. When the driver is disabled, or when VDD is powered down, Pin Z is put into a high impedance state to avoid overloading the bus.
11	B	Inverting Receiver Input.
12	A	Noninverting Receiver Input.
13	VDD	Power Supply.
14	VDD	Power Supply.

2. Absolute Maximum Ratings

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Power Supply Voltage	VDD	-0.5		6	V	
Maximum Input Voltage	/RE, DE, D	-0.4		VDD+0.4	V	
Driver Output/Receiver Input Voltage	VA, VB, VY, VZ	-7		12	V	
Differential input voltage, A with repect to B	V_{ID}	-18		18	V	
Receiver Output Current	Io	-15		15	mA	
Operating Temperature	Topr	-40		125	℃	
Storage Temperature	Tstg	-40		150	℃	
Electrostatic discharge	HBM (Bus pins and GND)			±8000	V	
	HBM (All pins)			±6000	V	
	CDM			±2000	V	

3. Thermal Information

Parameters	Symbol	SOP8	SOP14	Unit
IC Junction-to-Air Thermal Resistance	θ_{JA}	67.9	86.4	℃/W
Junction-to-case (top) thermal resistance	$\theta_{JC（top）}$	27.7	43.7	℃/W
Junction-to-board thermal resistance	θ_{JB}	29.4	42.5	℃/W

4. Specifications

4.1. DC Electrical characteristics

(VDD=3.0V~5.5V, Ta=–40℃ to 125℃. Unless otherwise noted, Typical values are at VDD = 5V Ta = 25℃)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Power supply voltage	VDD	3.0		5.5	V	
Logic-side supply current	I_{DD}		600	900	uA	DE=high, /RE=low, no load
			520	800	uA	DE=high, /RE=high, no load
			540	700	uA	DE=low, /RE=low, no load
			0.5	10	uA	DE=low, /RE=high, no load
Thermal-Shutdown Threshold	T_{TS}		165		℃	
Thermal-Shutdown Hysteresis	T_{TSH}		15		℃	
Logic Side						
Input High Voltage	V_{IH}	2			V	DE, D, /RE
Input Low Voltage	V_{IL}			0.8	V	DE, D, /RE
Input Current	I_{IN}	-2		2	uA	DE, D, /RE
Output Voltage High	V_{OH}	VDD-0.4			V	I_{OH} = -4mA
Output Voltage Low	V_{OL}			0.4	V	I_{OL} = 4mA
Output Short-Circuit Current	I_{OSR}	-150		150	mA	$0 \le V_R \le VDD$
Three-State Output Current	I_{OZ}			1	uA	$0 \le V_R \le VDD$, /RE = high
Driver						
Differential Output Voltage	$\|V_{OD}\|$			VDD	V	No Load
		2.7		VDD	V	See Figure 4.2, R_L=100Ω (RS-422), VDD=5V
		1.5		VDD	V	See Figure 4.2, R_L=100Ω (RS-422), VDD=3.3V
		2.1		VDD	V	See Figure 4.2, R_L=54Ω (RS-485), VDD=5V
		1.3		VDD	V	See Figure 4.2, R_L=54Ω (RS-485), VDD=3.3V
Change in magnitude of the differential output voltage	$\Delta\|V_{OD}\|$			0.2	V	See Figure 4.2, R_L=100Ω or R_L=54Ω
Common-Mode Output Voltage	$\|V_{OC}\|$		VDD/2		V	See Figure 4.2, R_L=100Ω or R_L=54Ω

Change in Magnitude of Common-Mode Voltage	Δ|V$_{OC}$|			0.2	V	See Figure 4.2, R$_L$=100Ω or R$_L$=54Ω
Driver Short-Circuit Output Current	I$_{OSD}$			250	mA	0 ≤ V$_{OUT}$ ≤ +12 V
		-250			mA	−7V ≤ V$_{OUT}$ ≤ VDD
Output Leakage Current (Y and Z) Full-Duplex	I$_O$			200	uA	DE=GND, VIN=12V
		-150			uA	DE=GND, VIN=-7V
Receiver						
Input Current (A and B)	I$_A$, I$_B$			200	uA	DE=GND, VDD=GND, V$_{IN}$=12V
		-200			uA	DE=GND, VDD=GND, V$_{IN}$=-7V
Receiver Differential Threshold Voltage	V$_{TH}$	-200	-125	-10	mV	−7V ≤ V$_{CM}$ ≤ 12V
Receiver Input Hysteresis	ΔV$_{TH}$		15		mV	V$_A$+V$_B$=0
Receiver Input Resistance	R$_{IN}$	96			kΩ	−7V ≤ V$_{CM}$ ≤ 12V, DE=low

4.2. Switching Electrical Characteristics

(VDD=3.0V~5.5V, Ta=−40℃ to 125℃. Unless otherwise noted, Typical values are at VDD = 5V Ta = 25℃)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Driver						
Maximum Data Rate	f_{MAX}	12			Mbps	
Driver Propagation Delay	t_{PLH}		30	50	ns	See Figure 4.3，R_L=54Ω，C_L=50pF
	t_{PHL}		30	50	ns	See Figure 4.3，R_L=54Ω，C_L=50pF
Driver Pulse Width Distortion, |t_{PHL} − t_{PLH}|	PWD		1		ns	See Figure 4.3，R_L=54Ω，C_L=50pF
Driver Output Falling Time or Rising time	t_F		8		ns	See Figure 4.3，R_L=54Ω，C_L=50pF
	t_R		7		ns	See Figure 4.3，R_L=54Ω，C_L=50pF
Driver Enable to Output High	t_{ZH}		17.2	60	ns	Receiver enabled, See Figure 4.4，R_L=110Ω，C_L=50pF
			500	900	ns	Receiver disabled, See Figure 4.4，R_L=110Ω，C_L=50pF
Driver Enable to Output Low	t_{ZL}		26.8	60	ns	Receiver enabled, See Figure 4.4，R_L=110Ω，C_L=50pF
			500	900	ns	Receiver disabled, See Figure 4.4，R_L=110Ω，C_L=50pF
Driver Output High to Disable	t_{HZ}		17	60	ns	See Figure 4.4，R_L=110Ω，C_L=50pF
Driver Output Low to Disable	t_{LZ}		24	60	ns	See Figure 4.4，R_L=110Ω，C_L=50pF
Receiver						
Maximum Data Rate	f_{MAX}	12			Mbps	
Receiver Propagation Delay	t_{PLH}		76	120	ns	See Figure 4.5，C_L=15pF
	t_{PHL}		78	120	ns	See Figure 4.5，C_L=15pF
Receiver Pulse Width Distortion	PWD		4		ns	|t_{PHL} − t_{PLH}|,See Figure 4.5，C_L=15pF

Receiver Output Falling Time or Rising time	t_F		2.4		ns	See Figure 4.5，C_L=15pF
	t_R		3.4		ns	See Figure 4.5，C_L=15pF
Receiver Enable to Output High	t_{ZH}		16	60	ns	Driver enabled, See Figure 4.6，R_L=1kΩ，C_L=15pF
			200	1400	ns	Driver disabled, See Figure 4.6，R_L=1kΩ，C_L=15pF
Receiver Enable to Output Low	t_{ZL}		16	60	ns	Driver enabled, See Figure 4.6，R_L=1kΩ，C_L=15pF
			200	1400	ns	Driver disabled, See Figure 4.6，R_L=1kΩ，C_L=15pF
Receiver Disable to Output High	t_{HZ}		17	60	ns	See Figure 4.6，R_L=1kΩ，C_L=15pF
Receiver Disable to Output Low	t_{LZ}		14	60	ns	See Figure 4.6，R_L=1kΩ，C_L=15pF
Shutdown time	t_{SD}	80		5000	ns	

4.3. Typical Performance Characteristics
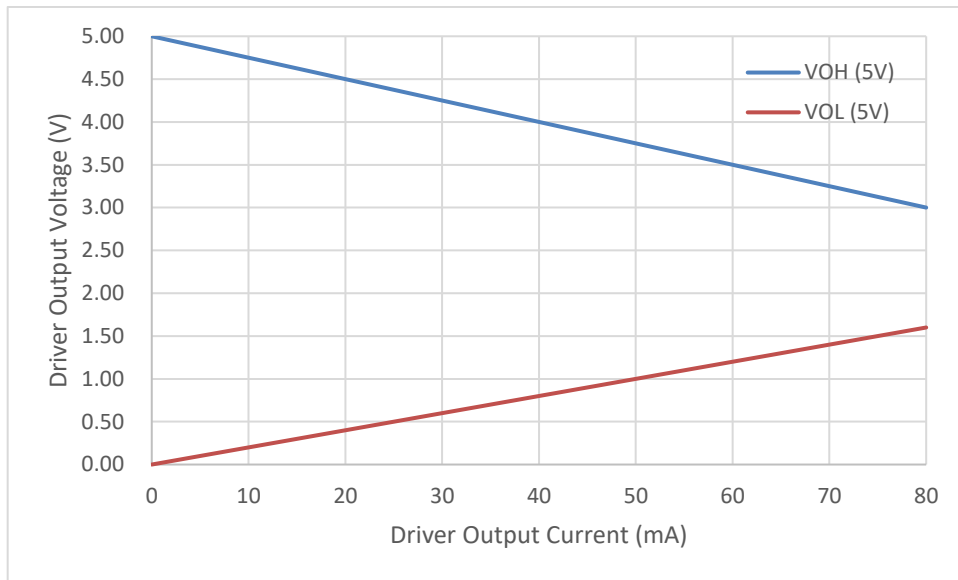
Figure 4.1 Receiver output voltage vs Output current

4.4. Parameter Measurement Information
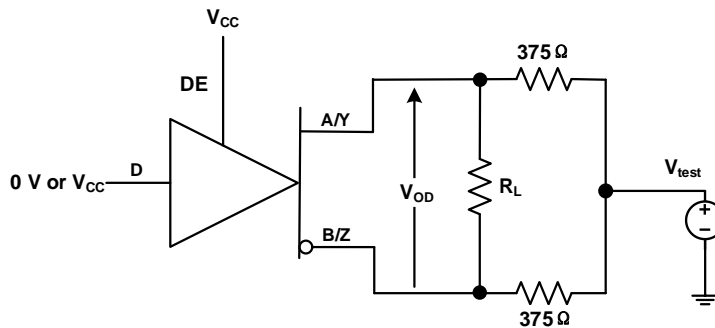
Figure 4.2 Driver DC Test Load
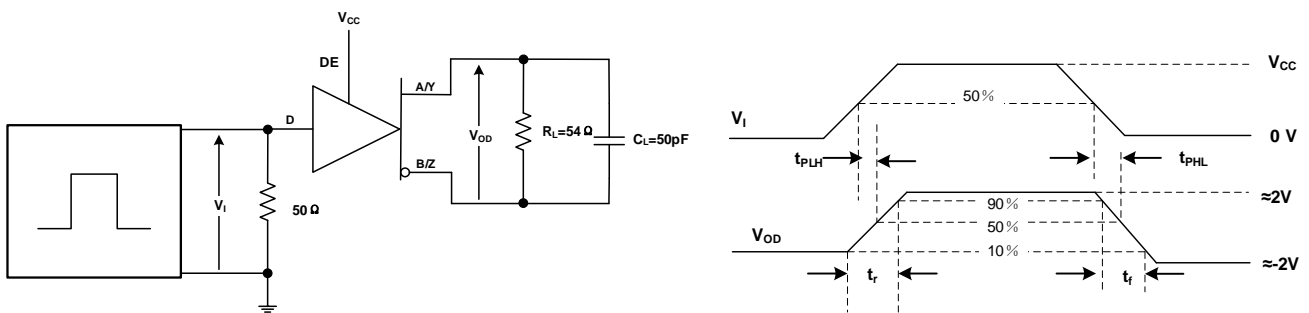
Figure 4.3 Driver Timing Test Circuit and waveform
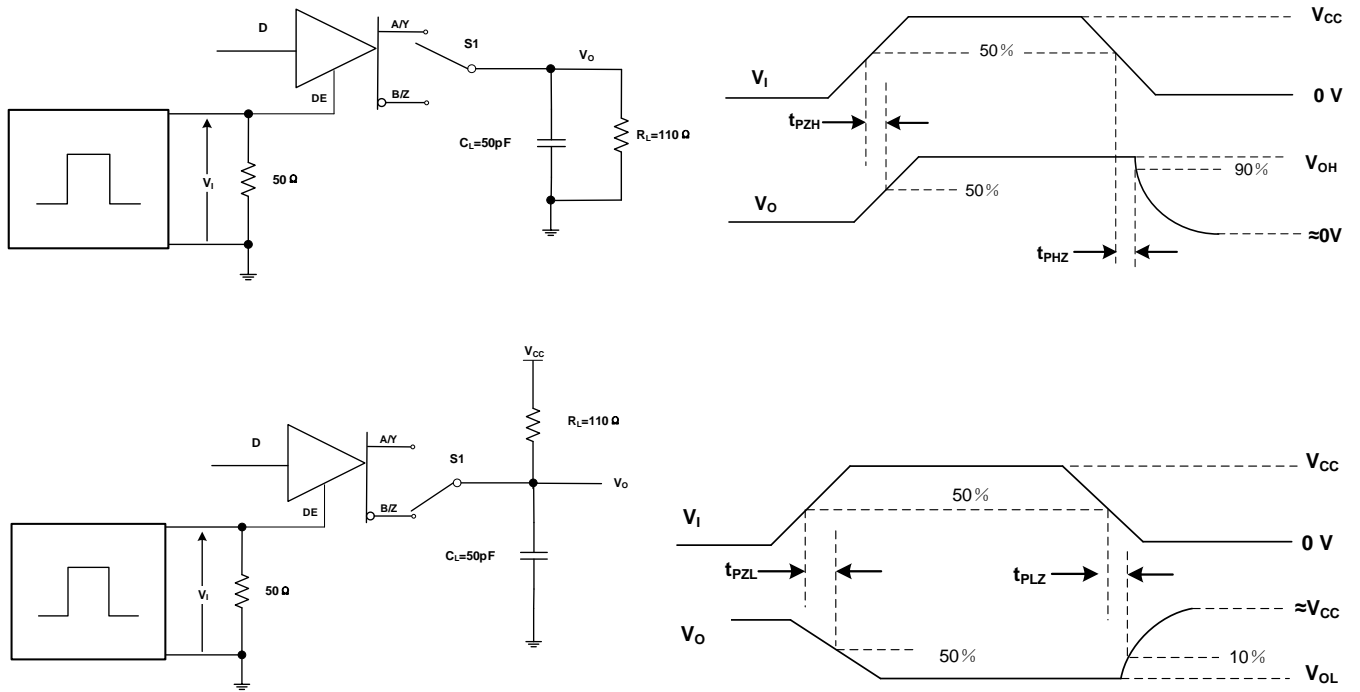
Figure 4.4 Driver Enable or Disable Timing Test Circuit and waveform
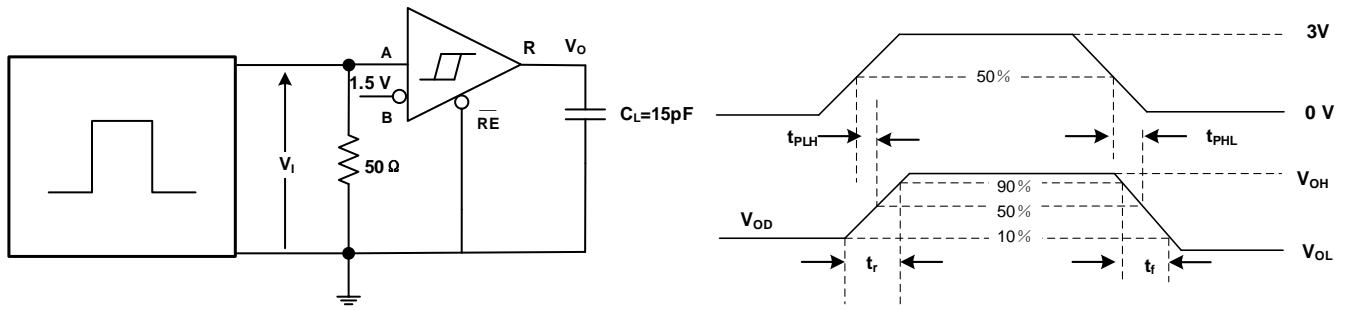
Figure 4.5 Receiver Propagation Delay Test Circuit and waveform
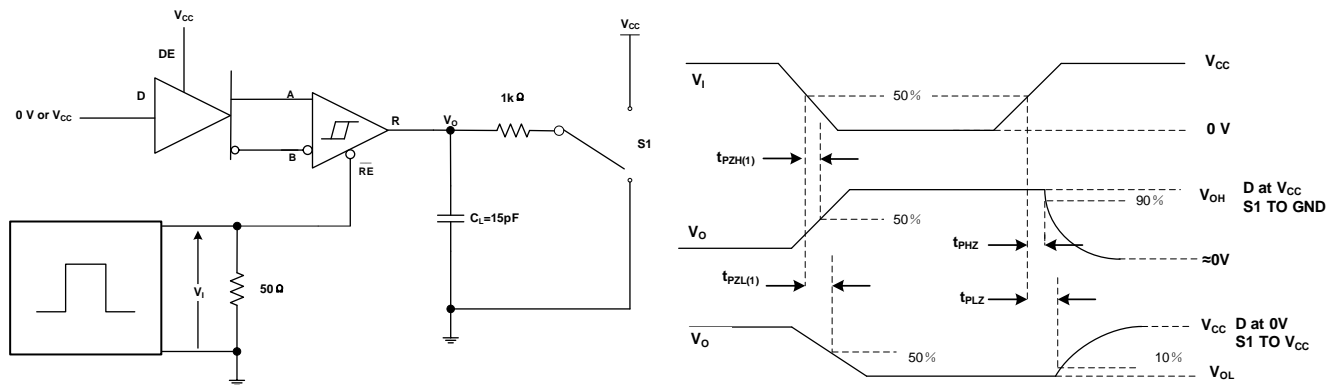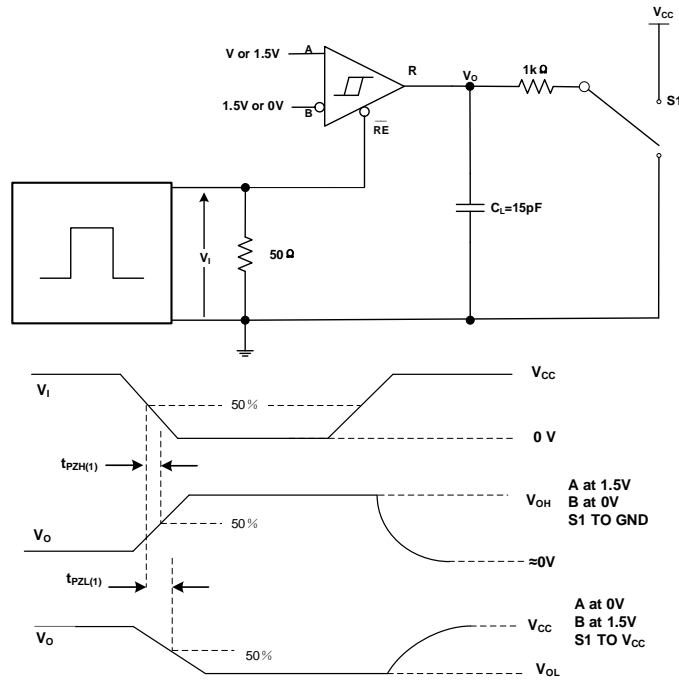
Figure 4.6 Receiver Enable or Disable Timing Test Circuit and waveform

5. Function Description

5.1. Data rate

The data rate of NCA3485/NCA3491 is 12Mbps. The device is slew limited to reduce EMI and reflections with improperly terminated transmission line.

5.2. True Fail-safe receiver inputs

The devices feature fail-safe circuitry, which guarantees a logic-high receiver output when the receiver inputs are open or shorted. The receiver threshold is fixed between -10mV and -200mV, which meets EIA/TIA-485 standard. If the differential input voltage (V_A-V_B) is greater than or equal to -10mV, receiver output R is logic high. In the case of a terminated bus with all transmitters disabled, the differential input voltage is pulled to zero by the termination resistors. Due to the receiver threshold, the receiver output R is logic high.

5.3. Truth tables

Table 5.1 Driver Function Table[1]

Input (D)	Enable Input (DE)	Outputs[1]	
		A/Y	B/Z
H	H	H	L
L	H	L	H
X	L	Z	Z
X	OPEN	Z	Z
OPEN	H	L	H

[1] PD= Powered down; PU= Powered up; H= Logic High; L= Logic Low; X= Irrelevant; Z= High Impedance.

Table 5.2 Receiver Function Table[1]

Differential Input (V_A-V_B)	Enable Input (/RE)	Output (R)
≥-10mV	L/Open	H
≤-200mV	L/Open	L
Open/Short	L/Open	H
X	H	Z
Idle	L	H

[1] PD= Powered down; PU= Powered up; H= Logic High; L= Logic Low; X= Irrelevant; Z= High Impedance.

5.4. Thermal shutdown

The device is protected from over temperature damage by integrated thermal shutdown circuitry. When the junction temperature (TJ) exceeds +165°C (typ), the driver outputs go high-impedance. The device resumes normal operation when TJ falls below +145°C (typ).

6. Application Note

6.1. 256 transceivers on the bus

The devices have a 1/8-unit-load receiver input impedance (96kΩ) that allows up to 256 transceivers on the bus. Connect any combination of these devices, and/or other RS-485 devices, for a maximum of 32 unit-loads to the line.

6.2. ESD protection

ESD protection structures are enhanced on all pins to protect against electrostatic discharge encountered during handing and assembly.

ESD protection can be tested in various ways. Below is the ESD spec of the devices.

Bus pins:

- ± 8kV HBM.

- ±10kV using the Contact Discharge method specified in IEC 61000-4-2

Other pins except bus pins:

- ±6kV HBM.

- ±7kV using the Contact Discharge method specified in IEC 61000-4-2

6.3. Layout considerations

The NCA3485 requires a 0.1 μF bypass capacitor between VDD and GND. The capacitor should be placed as close as possible to the package. To eliminate line reflections, each cable end is terminated with a resistor, whose value matches the characteristic impedance of the cable. It's good practice to have the bus connectors and termination resistor as close as possible to the A and B pins.

6.4. Typical application
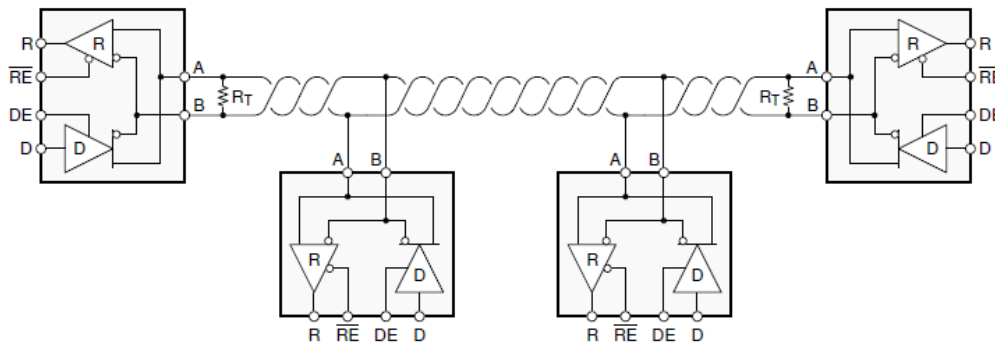
Figure 6.1 Typical Half-Duplex RS-485 application
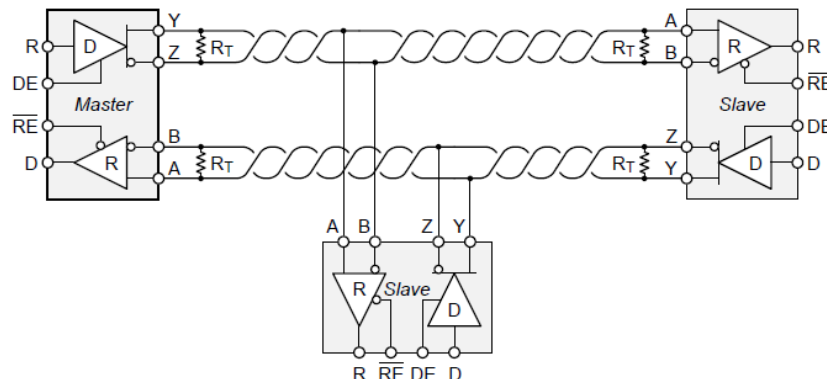
Figure 6.2 Typical Full-Duplex RS-485 application

7. Package Information
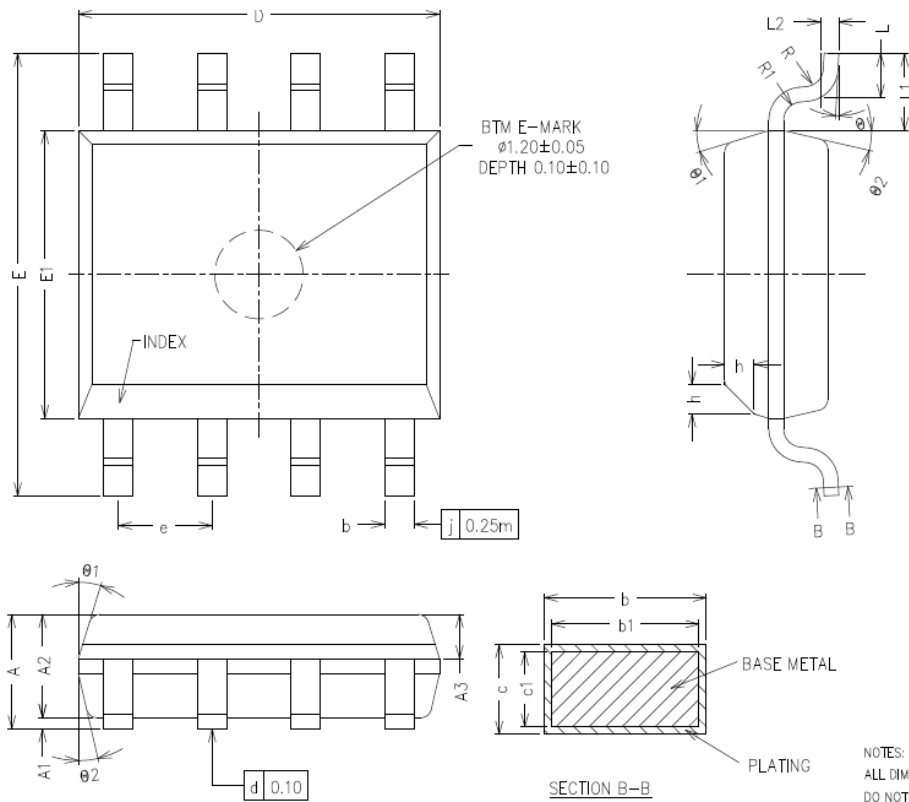
COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	1.35	1.55	1.75
A1	0.10	–	0.25
A2	1.30	1.40	1.50
A3	0.50	0.60	0.70
b	0.38	–	0.47
b1	0.37	0.40	0.43
c	0.17	–	0.25
c1	0.17	0.20	0.23
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.17	1.27	1.37
L	0.45	0.60	0.80
L1		1.04REF	
L2		0.25BSC	
R	0.07	–	–
R1	0.07	–	–
h	0.30	0.40	0.50
θ	0°	–	8°
θ1	15°	17°	19°
θ2	11°	13°	15°

ONLY FOR HFTF

NOTES:
ALL DIMENSIONS REFER TO JEDEC STANDARD MS−012 AA
DO NOT INCLUDE MOLD FLASH OR PROTRUSION.

Figure 7.1 SOP8 Package Shape and Dimension in millimeters
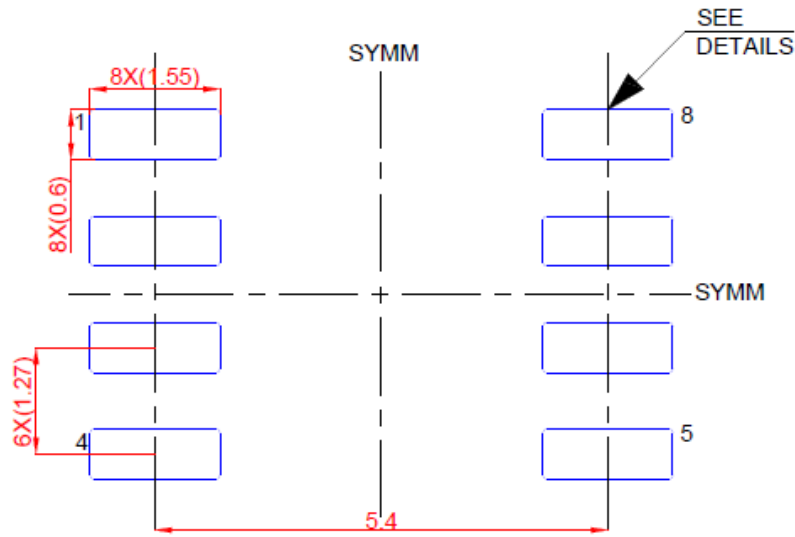
LAND PATTERN EXAMPLE(mm)
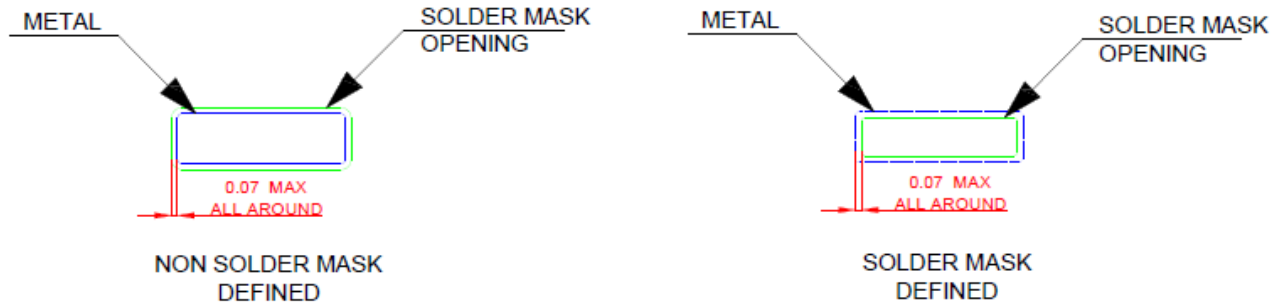
SOLDER MASK DETAILS

Figure 7.2 SOP8 Package Board Layout Example

Figure 7.3 SOP14 Package Shape and Dimension in millimeters
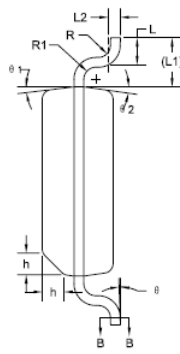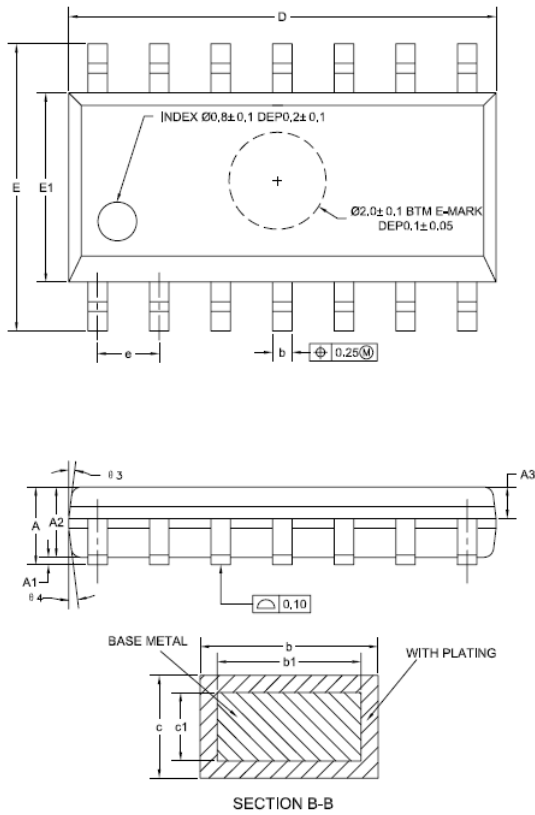
COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	1.35	1.60	1.75
A1	0.10	0.15	0.25
A2	1.25	1.45	1.65
A3	0.55	0.65	0.75
b	0.36	–	0.49
b1	0.35	0.40	0.45
c	0.17	–	0.25
c1	0.17	0.20	0.23
D	8.53	8.63	8.73
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e		1.27BSC	
L	0.45	0.60	0.80
L1		1.04REF	
L2		0.25BSC	
R	0.07	–	–
R1	0.07	–	–
h	0.30	0.40	0.50
θ	0°	–	8°
θ1	6°	8°	10°
θ2	6°	8°	10°
θ3	5°	7°	9°
θ4	5°	7°	9°

NOTES:
ALL DIMENSIONS MEET JEDEC STANDARD MS-012 AB
DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
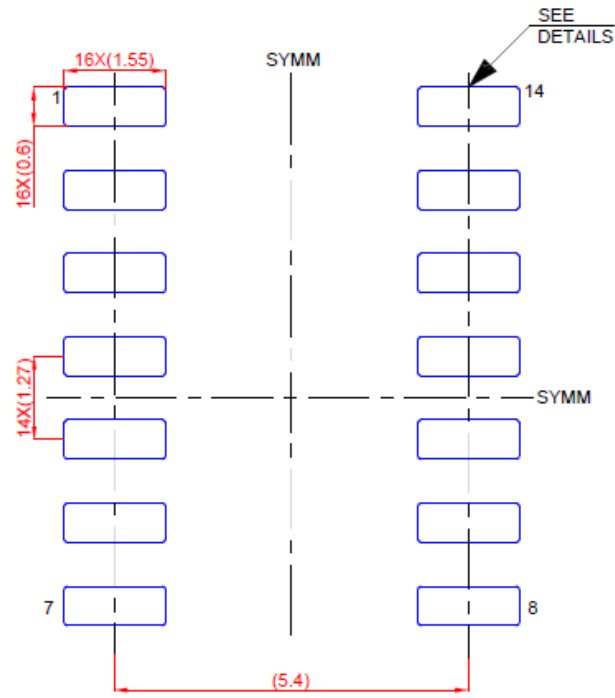
LAND PATTERN EXAMPLE(mm)

SOLDER MASK DETAILS

Figure 7.4 SOP14 Package Board Layout Example

8. Order Information

Part Number	Duplex	Max Data Rate (Mbps)	No. of Nodes	Temperature	MSL	Package Type	Package Drawing	SPQ
NCA3485-DSPR	Half	12	256	-40 to 125℃	3	SOP8 (150mil)	SOP8	2500
NCA3491-DSPKR	Full	12	256	-40 to 125℃	3	SOP14(150mil)	SOP14	2500
NOTE: All packages are RoHS-compliant with peak reflow temperatures of 260 ℃ according to the JEDEC industry standard classifications and peak solder temperatures.								

9. Documentation Support

Part Number	Product Folder	Datasheet	Technical Documents	Isolator selection guide
NCA3485	Click here	Click here	Click here	Click here
NCA3491	Click here	Click here	Click here	Click here

10. Tape and Reel Information
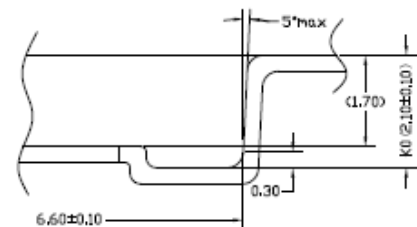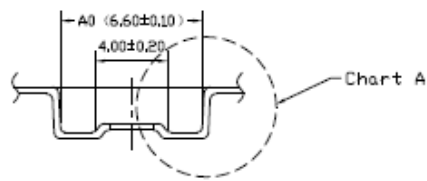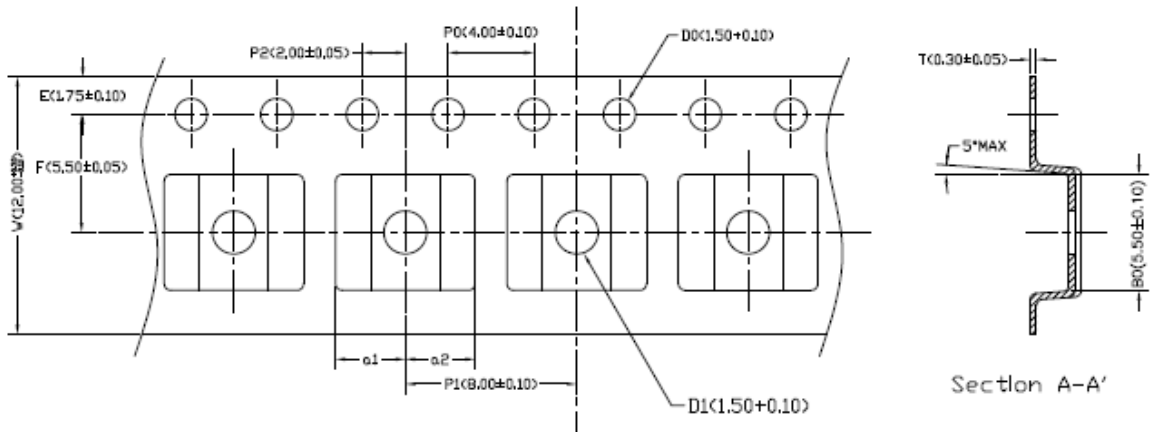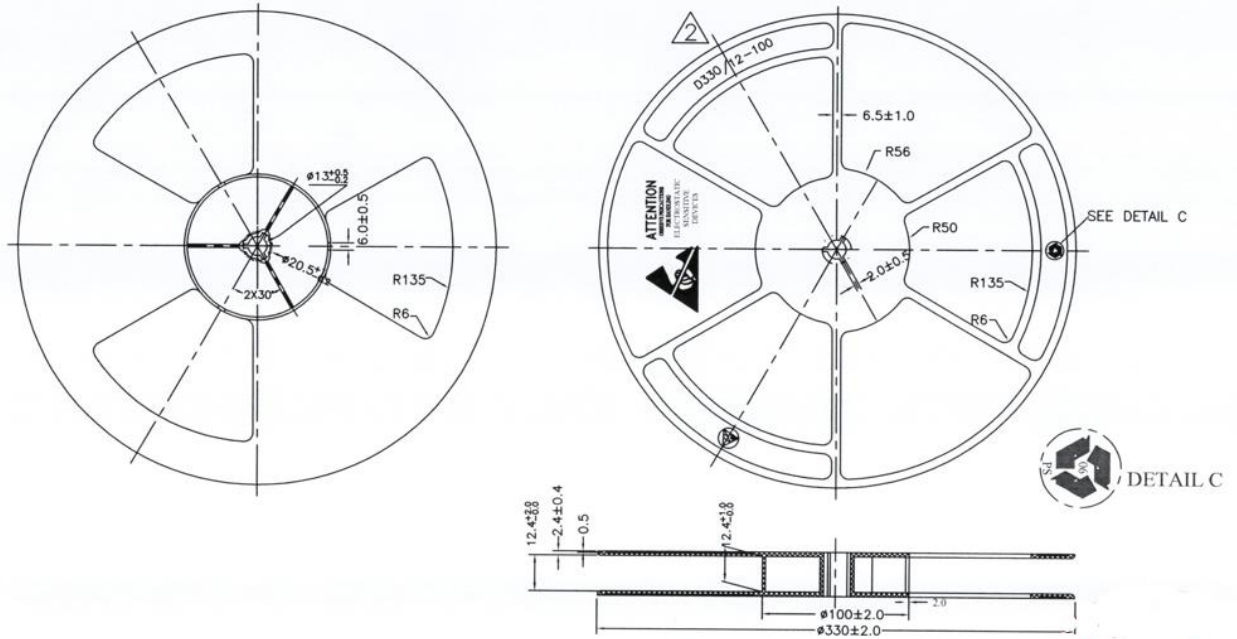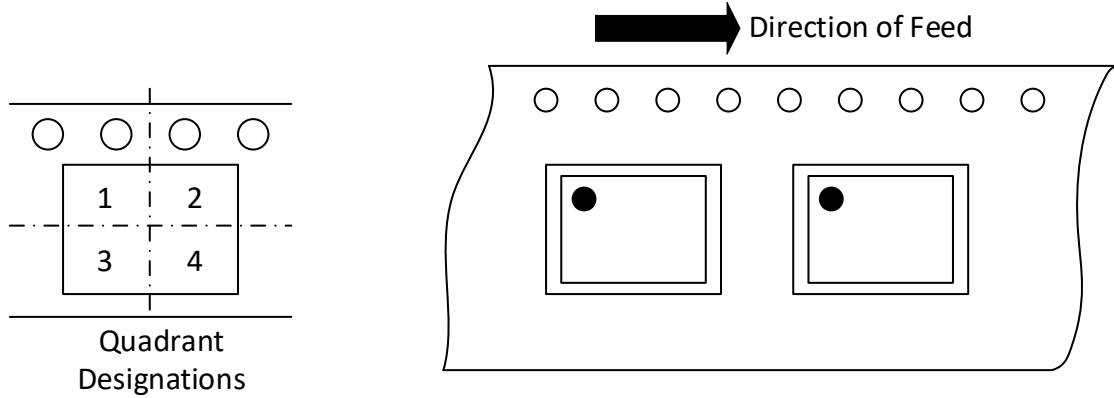
Figure 10.1 Tape and Reel Information of SOP8
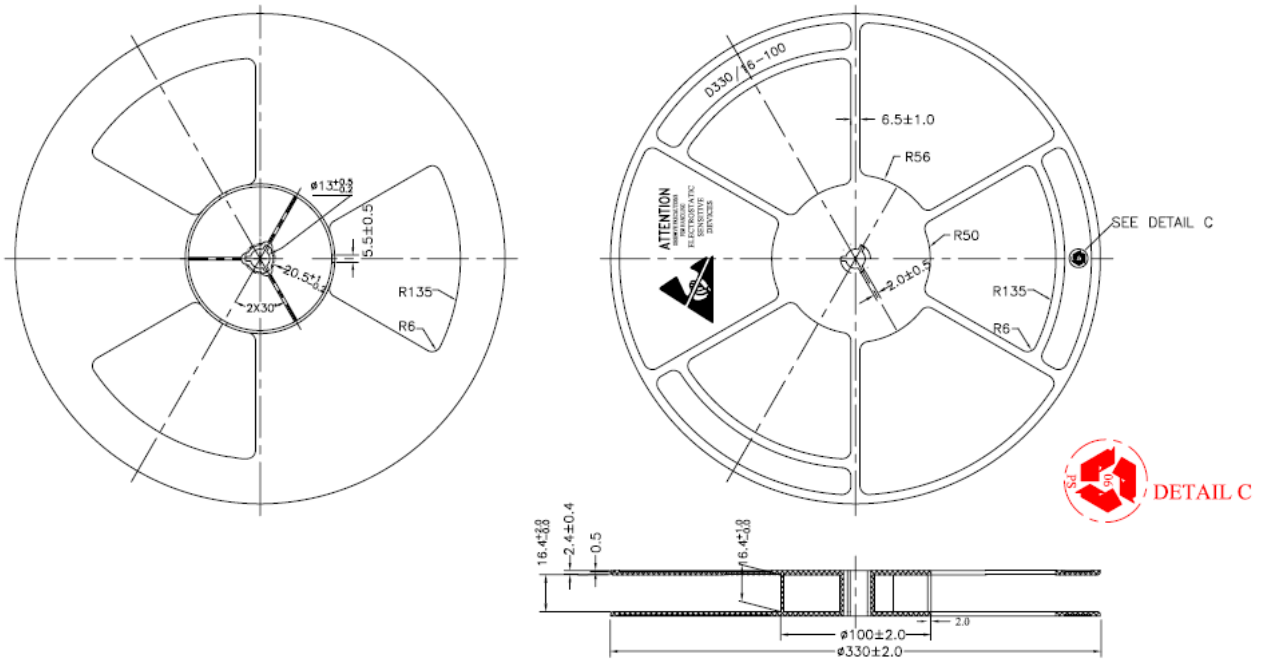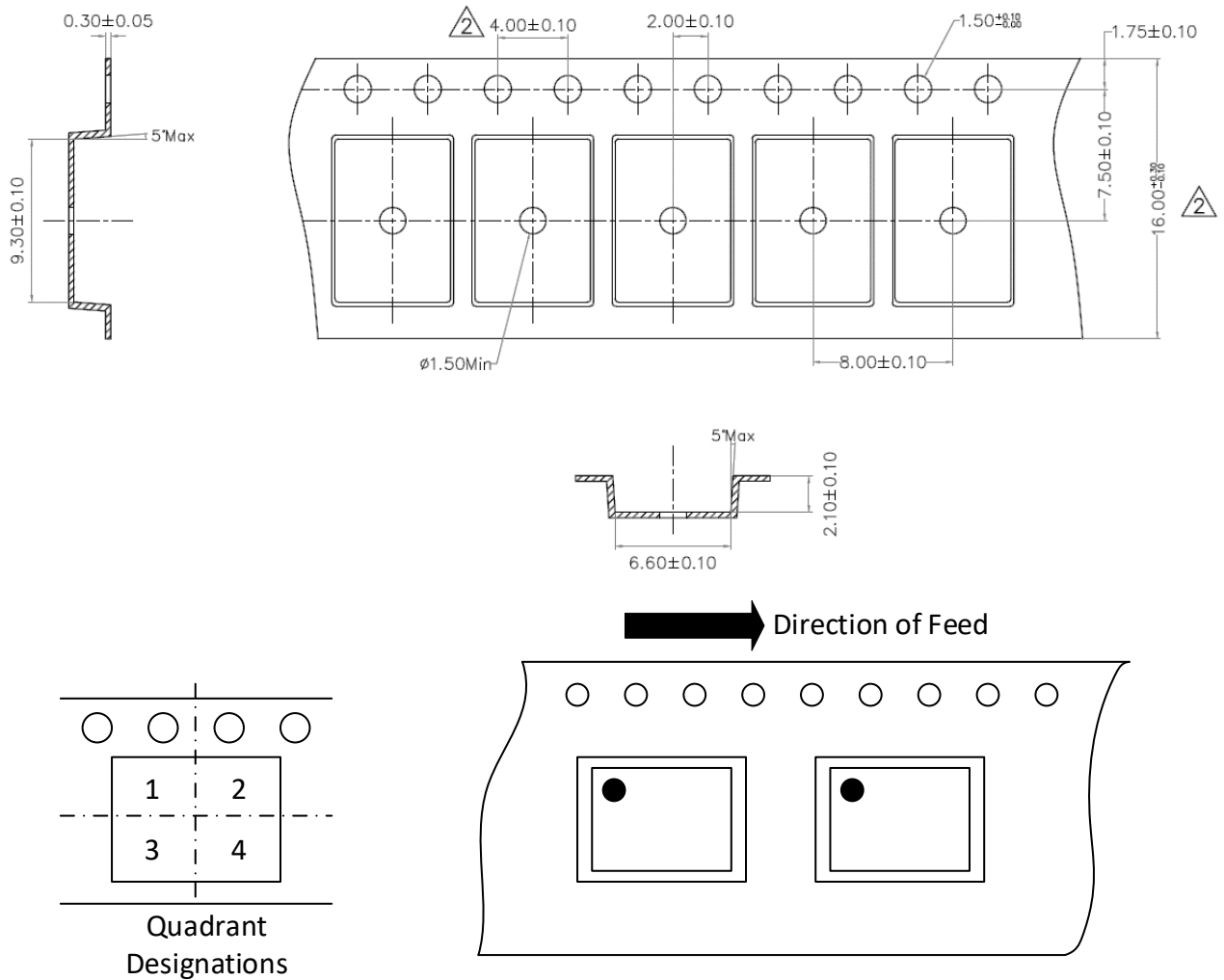
Figure 10.2 Tape and Reel Information of SOP14

11. Revision History

Revision	Description	Date
1.0	Initial version	2022/10/19
1.1	Changed the operation temperature	2023/3/6

IMPORTANT NOTICE